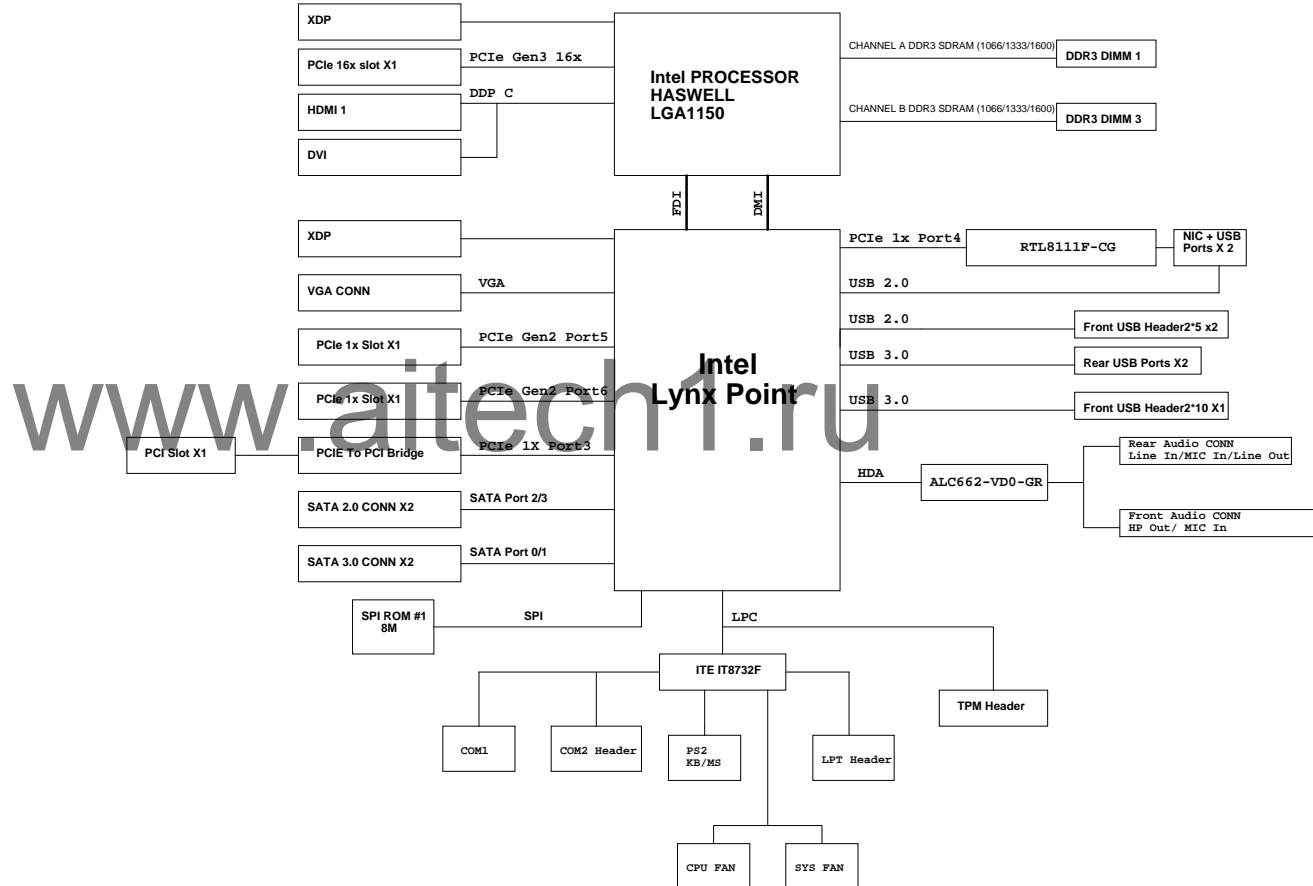


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FAB:A

1. Index / Block diagram
2. SMBus MAP
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30. FRONT USB2.0 Header
31. AUDIO ALC662
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33. SPI_Socket_ROM
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35. PS2/COM/LPT
36. FAN /TPM
37. ATX CONN/FP PANEL/EMI PART
38. Linear Power
39. 1.05V_PCH/ME
40. 5V_DUAL/3D3V_DUAL
41. V_SM
42. Vcore PWM
43. Vcore Driver

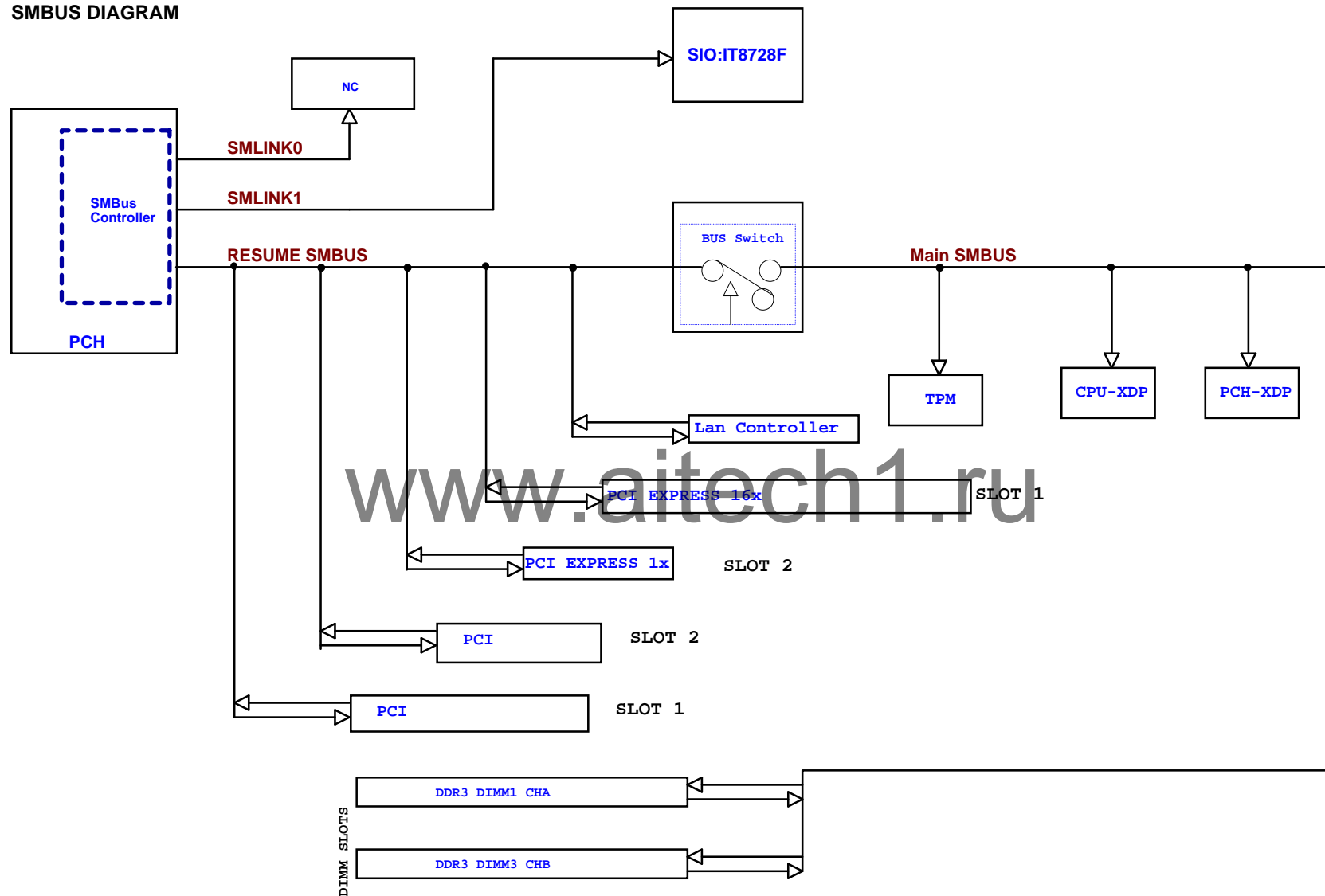


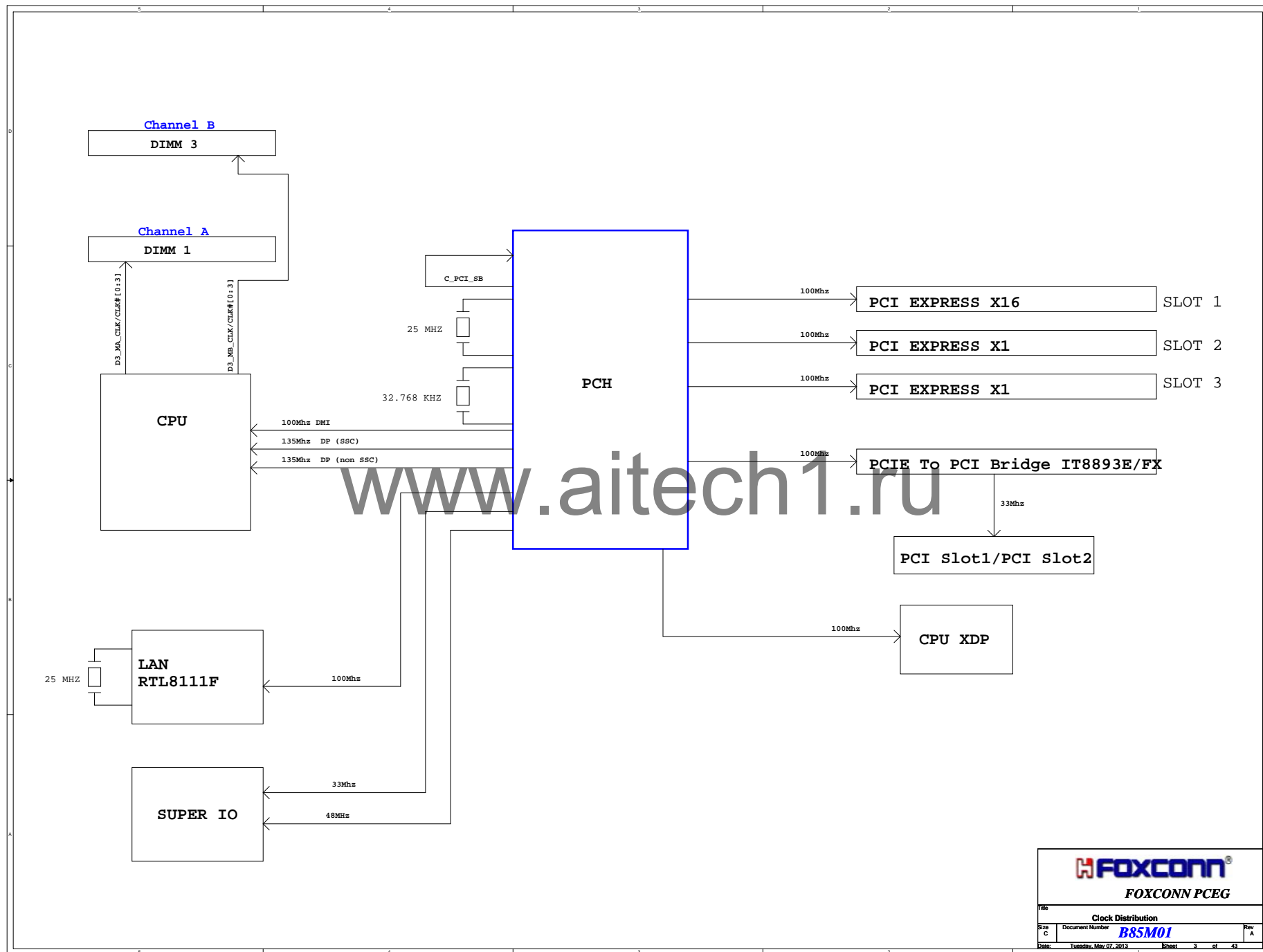
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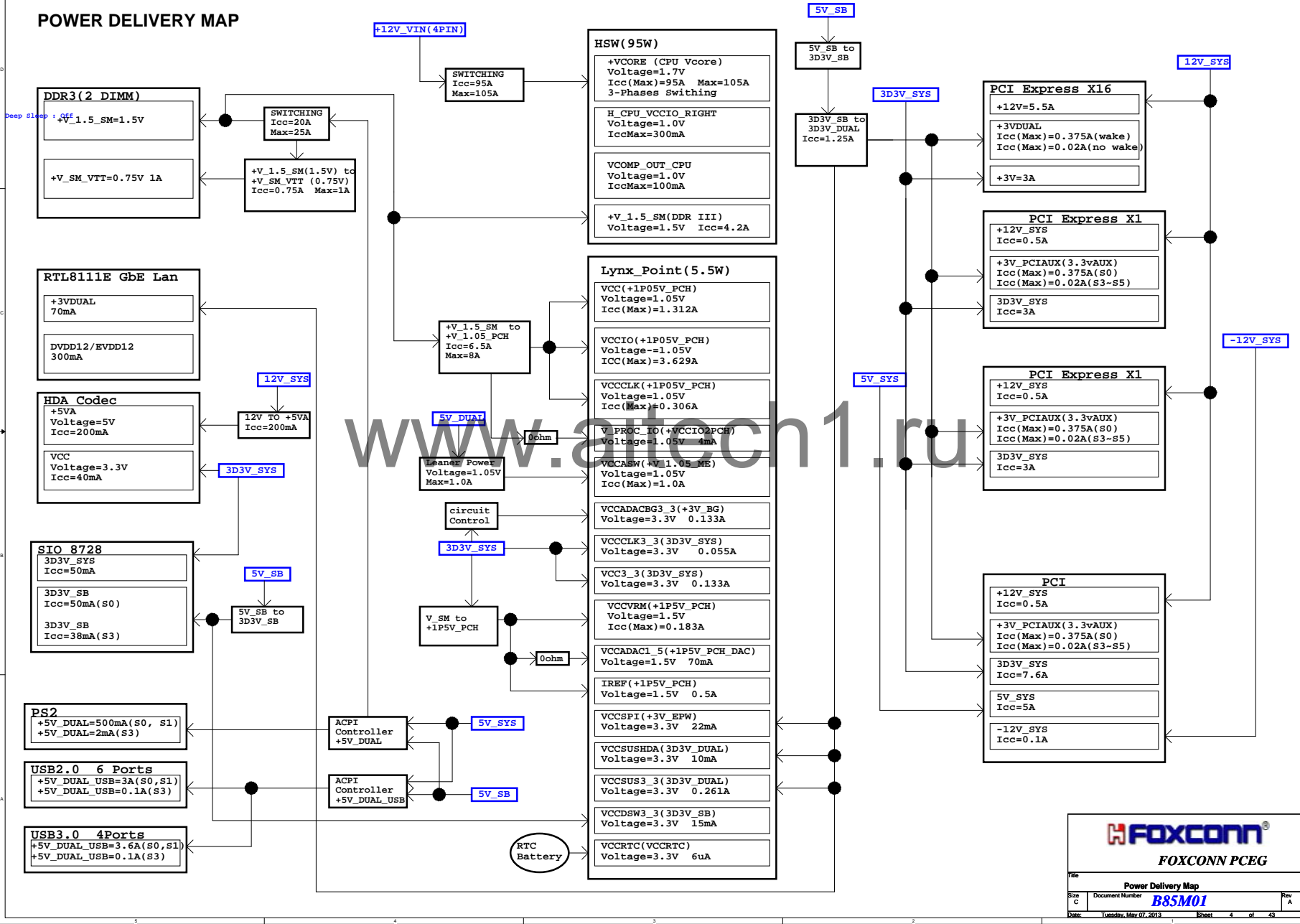
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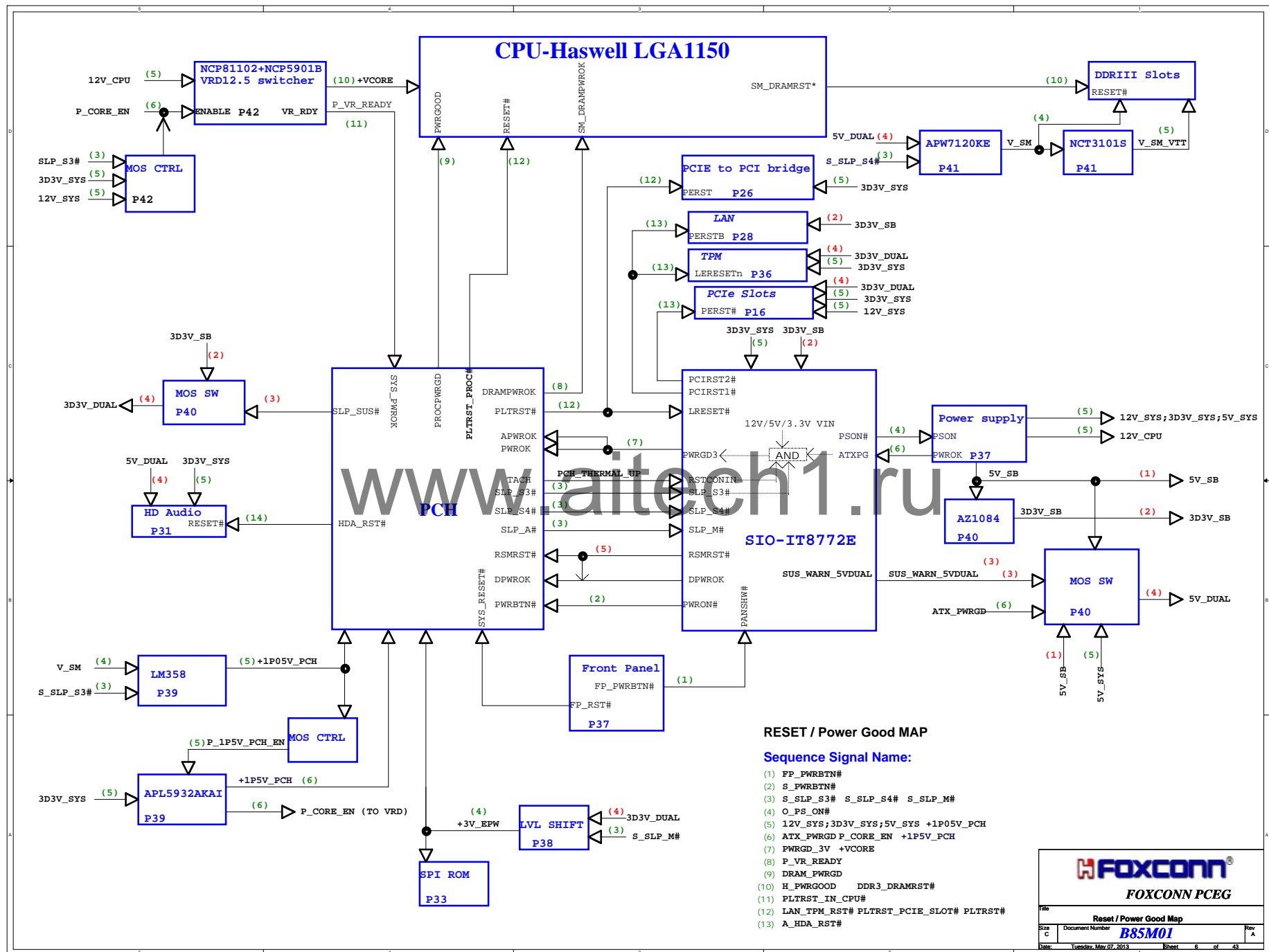
SMBUS DIAGRAM





POWER DELIVERY MAP





STRAPPING Table

CPU side

CFG[17:0]	Description	
[2]	PCI Express static x16 lane numbering reversal	1: normal Default 0: lane numbers reversed
[6:5]	PCI Express Bifurcation	00: 1x8, 2x4 PCI Express 01: reserved 10: 2x8 PCI Express 11: 1x16 PCI Express Default

Strapping Options Peak

Option	Strapping Options	Reason
0	0	Peak Cuts Resistor to VCC
1	1	Peak Cuts Resistor to VCC
2	2	Peak Cuts Resistor to VCC

Table 34-6. PCH Digital Display Strapping Signals

Checklist Item	Recommendations	Direction	Comments
DDPC_CTRLDATA	Straps for digital port B, C and D. For DisplayPort* - Should be pulled to 3.3V through a 2.2K W resistor to configure digital port. For DVI/HDMI configuration, the signal should be routed through the level shifter to the display connector. The signal is pulled to 3V before the level shifter and 5V before the display connector through a 2.2K W resistor. This signal should always be routed longer than DDPC_CTRLCLK by an inch. For DVI/HDMI configuration with the Cost Reduced level shifter, the signal should be routed through the pass gate sourced from 3.3V voltage. The signal is pulled to 3V before the pass gate and 5V before the display connector through a 2.2K W resistor and a Schottky diode. This signal should always be routed longer than DDPC_CTRLCLK by an inch. Also ensure schottky diode is not shared with DDPC_CTRLCLK.	BI	

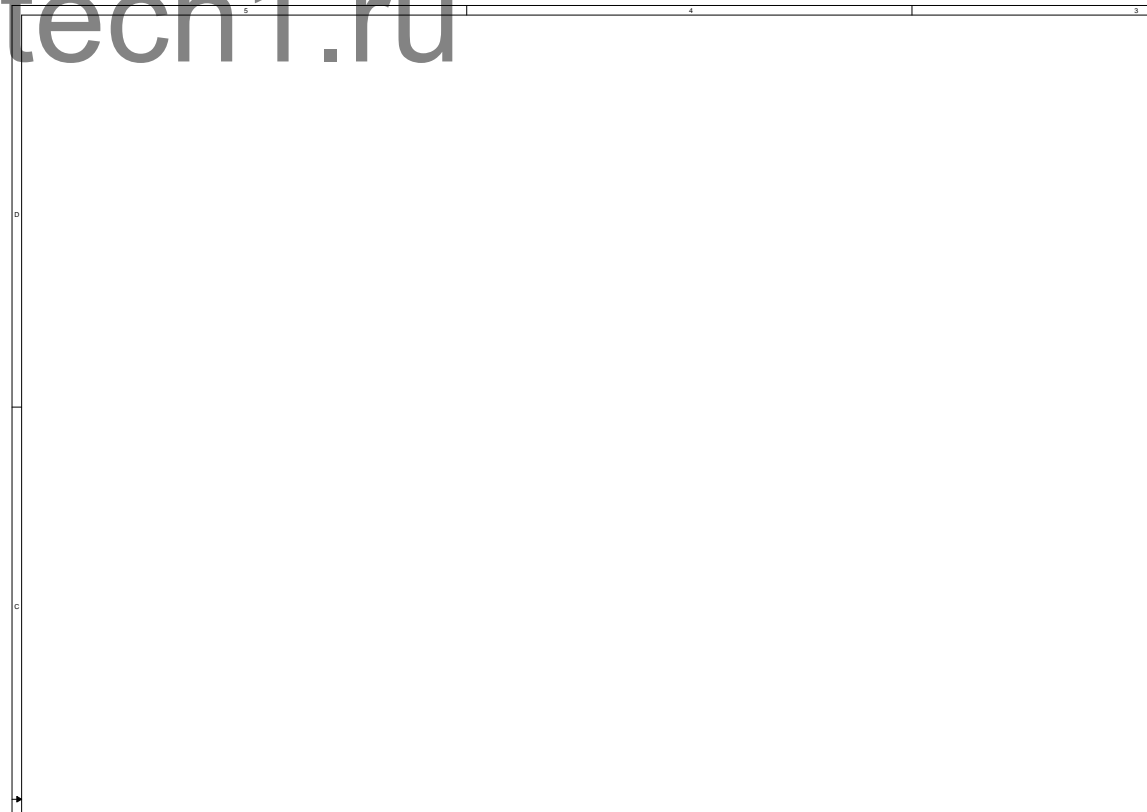
Table 36-18. Strapping Signals (Sheet 1 of 2)

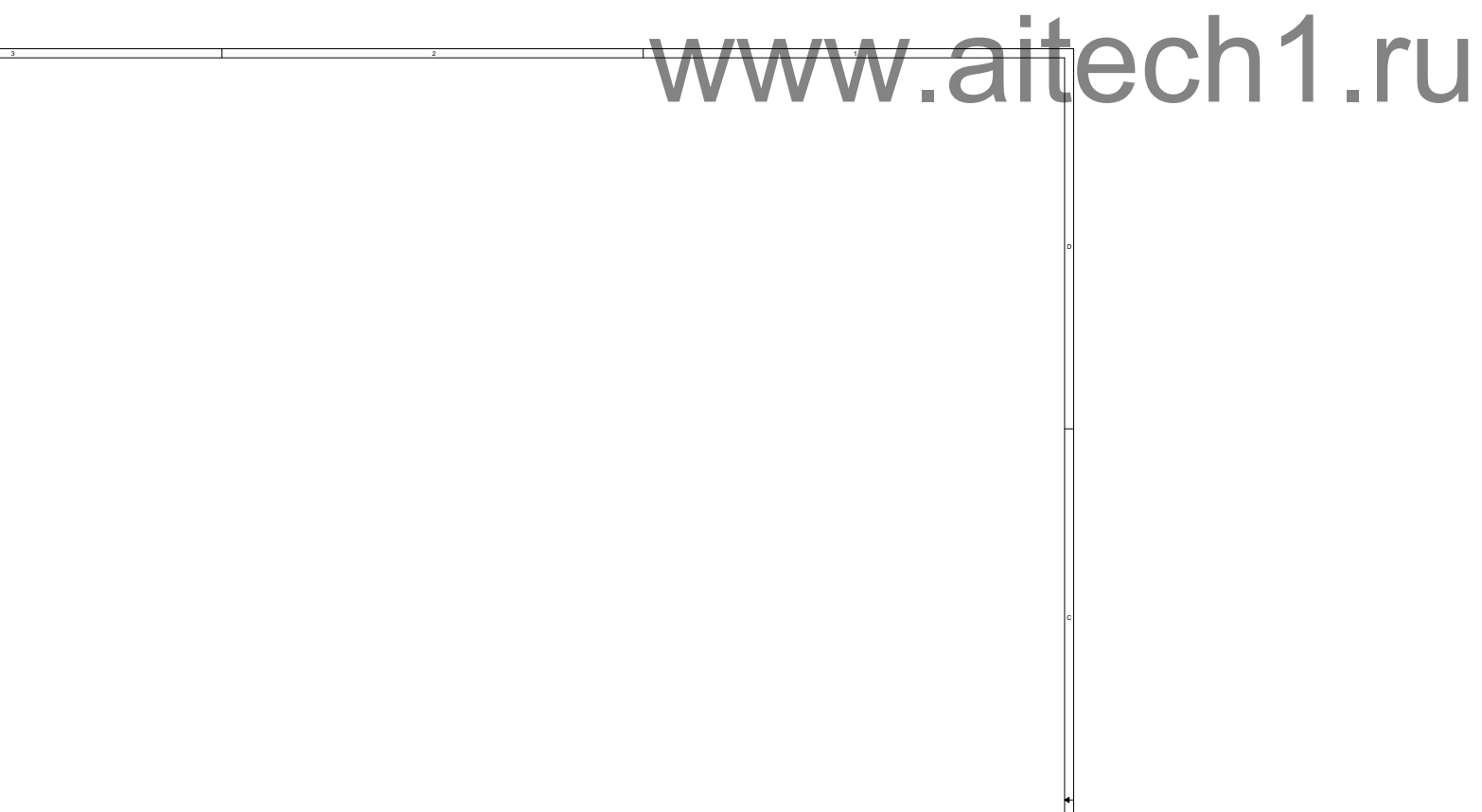
Name	Type	Recommendations	Reason/Impact
SPKR	I	Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2K-10K Ohm weak pull-up resistor.	
INIT3_3V#	I	Do not pull low.	
GPI055	I/O	Default Mode: Internal pull-up. Top Block Swap Mode: Connect to ground with 4.7K Ohm weak pull-down resistor.	
SATA1GP/ GPI019/ GPI051	I/O	Default (SPI) Left both SATA1GP/GPI019 and GPI051 floating. No pull up required. Boot from PCI Connect SATA1GP/GPI019 to ground with 1k Ohm pull-down resistor. Leave GPI051 Floating. Boot from LPC Connect both SATA1GP/GPI019 and GPI051 to ground with 1k Ohm pull-down resistor.	If LPC is selected BIOS may still be placed on LPC, but all platforms with PCH require SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. Booting to PCI is intended for debug/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or via Boot BIOS Destination Select will not affect SPI access initiated by Management Engine or Integrated GbE LAN. BI strap for server platform only.
GPI053	I/O	Do not pull low. Connect to ground with 1k Ohm pull-down resistor.	
HDA_SDO	I/O	Default Do not pull high. Disable ME in Manufacturing Mode Connect to VccSusHDA with 1k Ohm pull-up resistor through a jumper.	Flash descriptor Override
SPI_MOSI	I/O	Internal weak pull down.Do not pull high.	DMI RX Termination Voltage
SAAT3GP/ GPI037	I/O	Enable TLS: Pull up with 1k Ohm to VccSus3.3. Default (Disable TLS): Leave NC. Internal pull down.	TLS confidentiality
GPI08	I/O	Internal weak pull up.Do not pull low.	

Table 36-18. Strapping Signals (Sheet 2 of 2)

Name	Type	Recommendations	Reason/Impact
GPI062/ SUSCLK	I/O	Internal weak pull up. Do not pull low.	On die PLL voltage regulator
GPI036	I/O	Internal weak pull down. Do not pull high.	
DDPB_CTRL_DATA DDPC_CTRL_DATA DDPD_CTRL_DATA	I/O	Straps for digital ports B, C and D. For DisplayPort* - Should be pulled to 3.3V through a 2.2K ohms resistor to configure digital port. For DVI/HDMI configuration, the signal should be routed through the level shifter to the display connector. The signal is pulled to 3V before the level shifter and 5V before the display connector through a 2.2K ohms resistor. This signal should always be routed longer than DDPC_CTRLCLK by an inch. For DVI/HDMI configuration with the Cost Reduced level shifter, the signal should be routed through the pass gate sourced from 3.3V voltage to the display connector. The signal is pulled to 3V before the pass gate and 5V before the display connector through a 2.2K ohms resistor. This signal should always be routed longer than SDVO/DDPC_CTRLCLK by an inch.	

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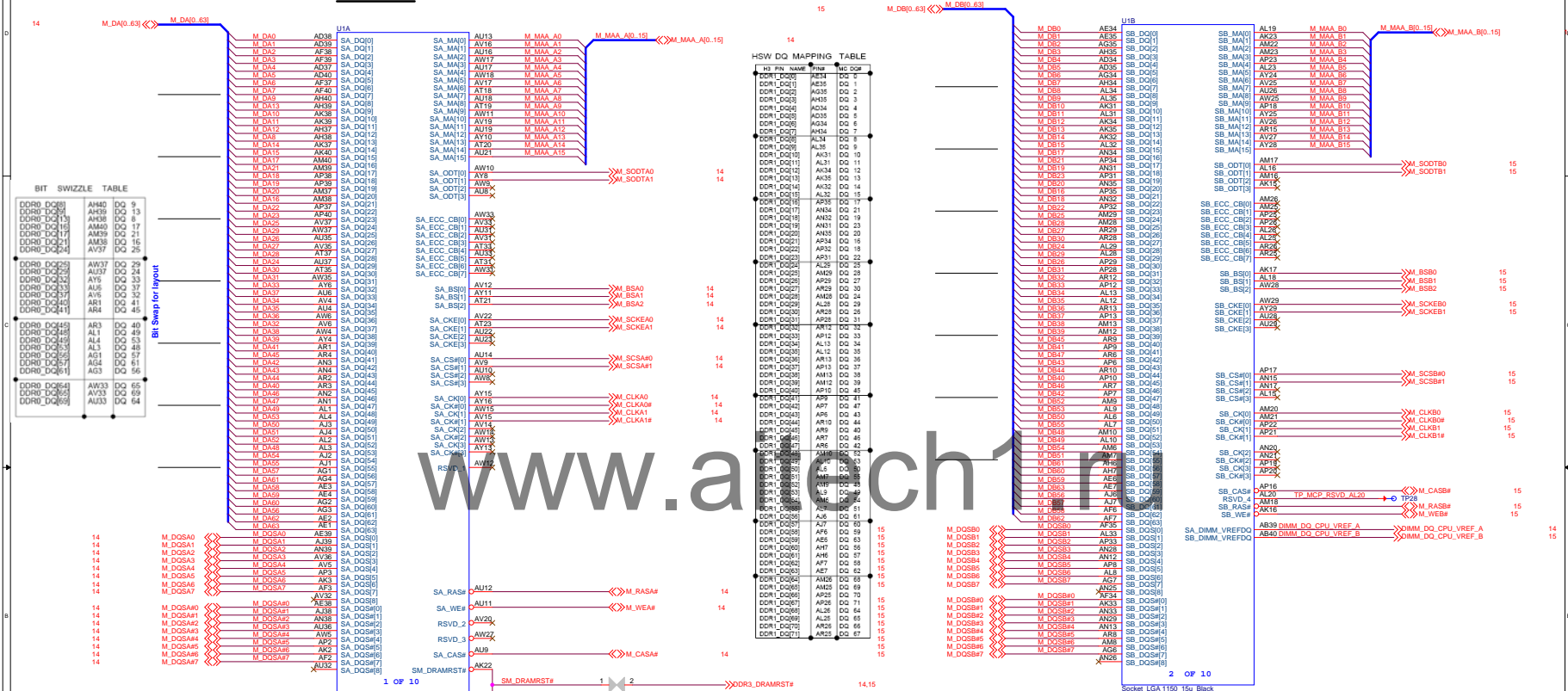
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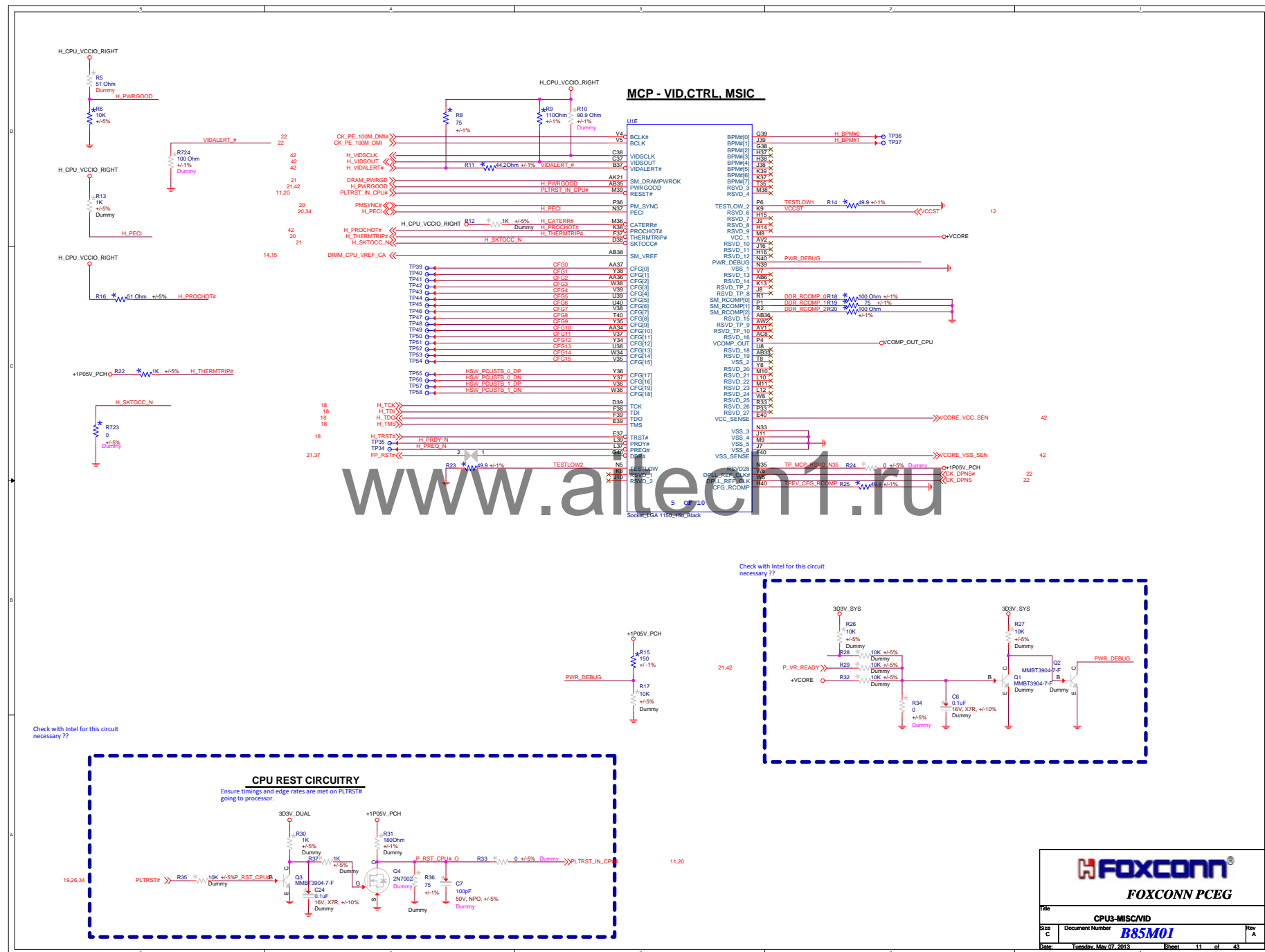
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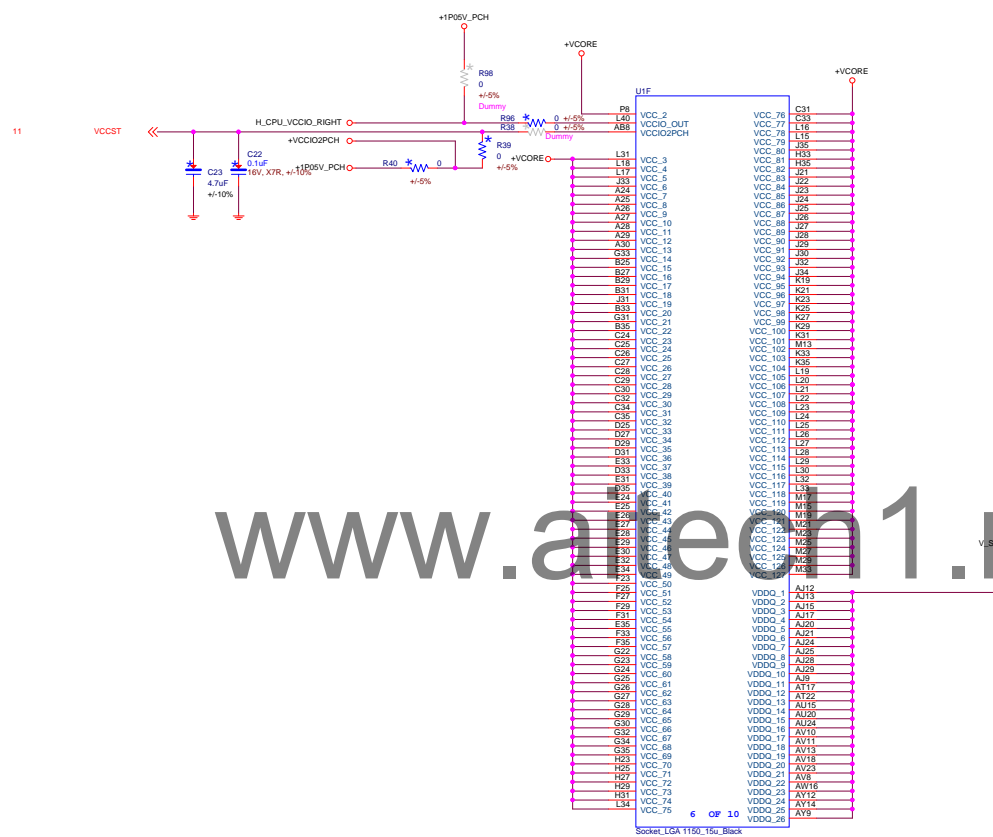
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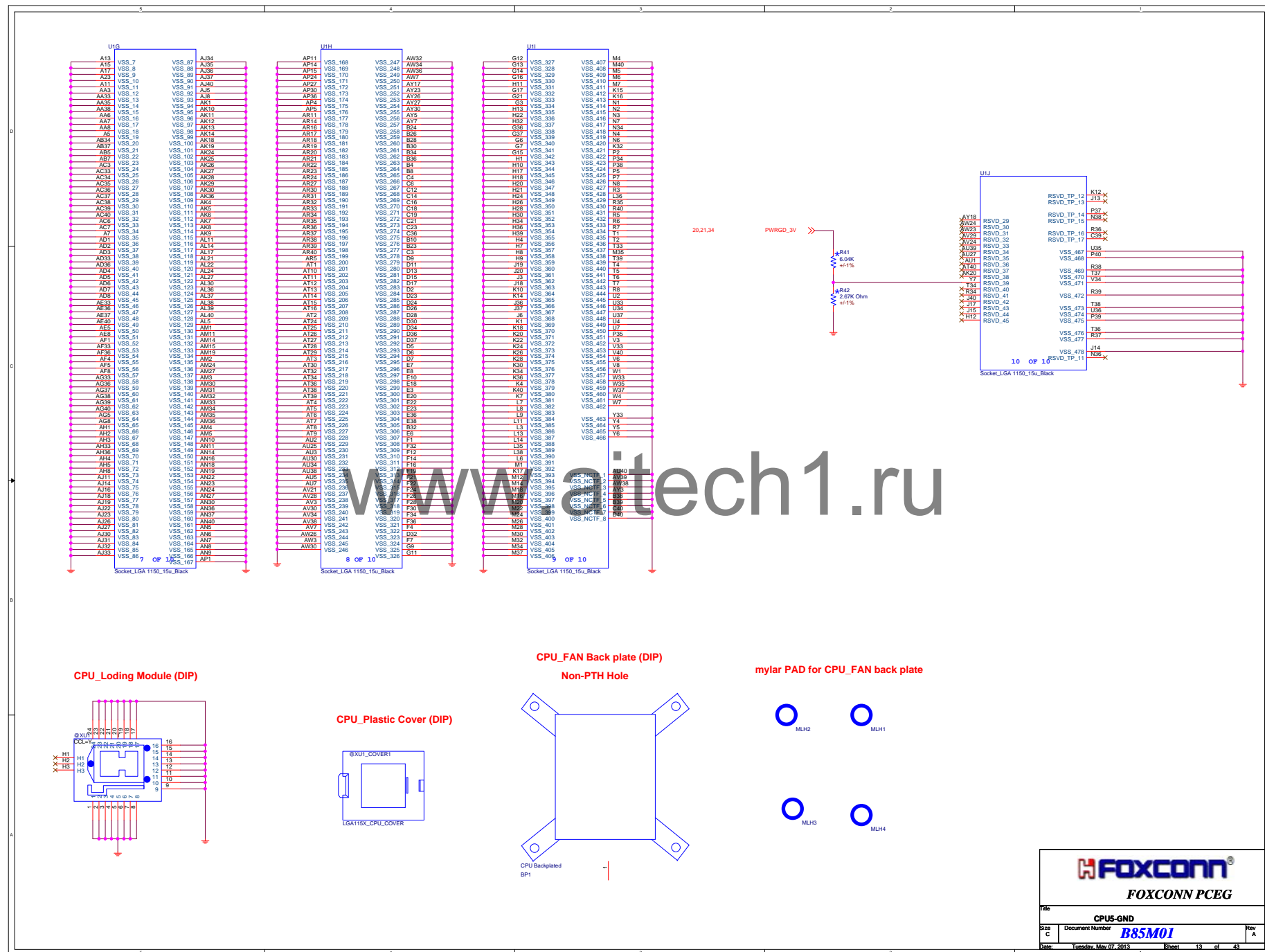


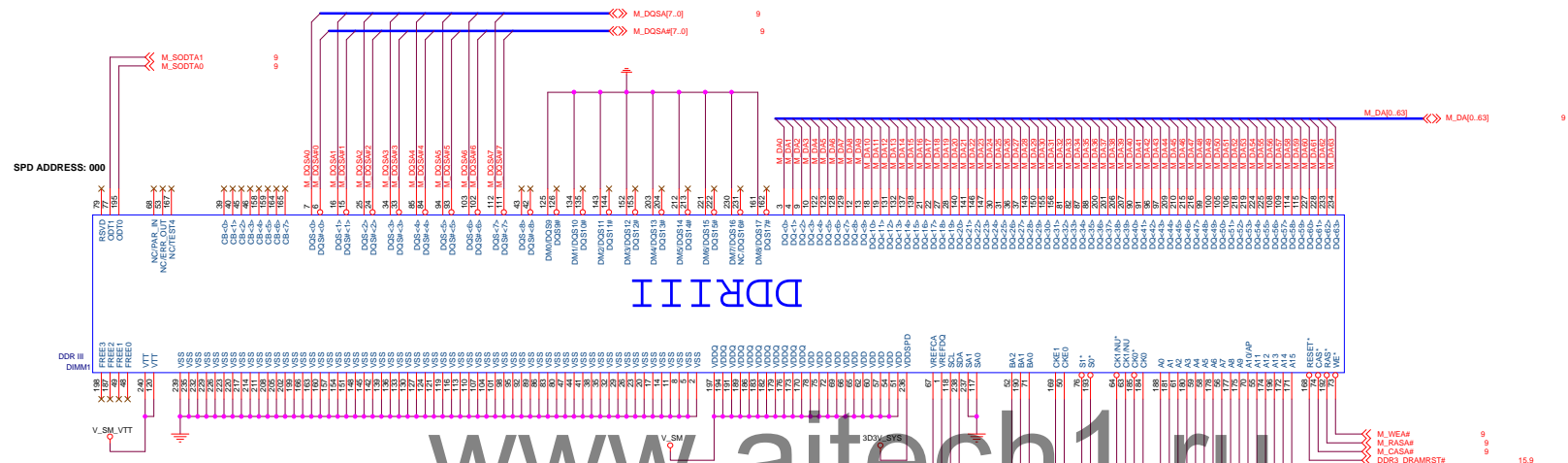
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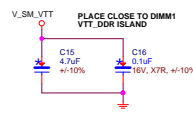
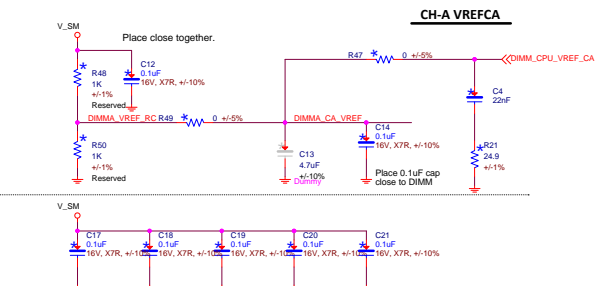
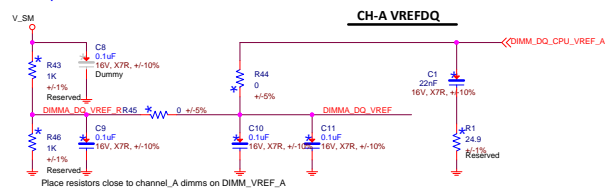








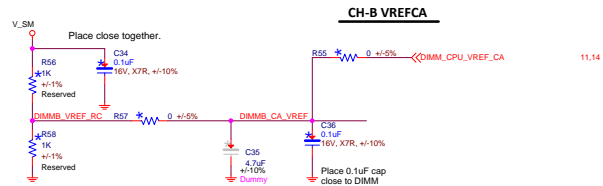
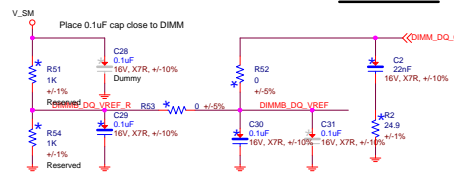
For future processor compatibility, the total on-board capacitance for VREFDQ per channel should be less than or equal to 0.3 Farads nominal



SPD ADDRESS: 010

DDR III

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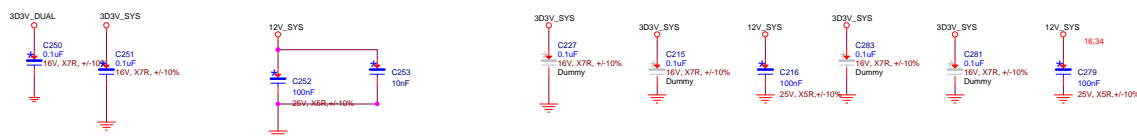
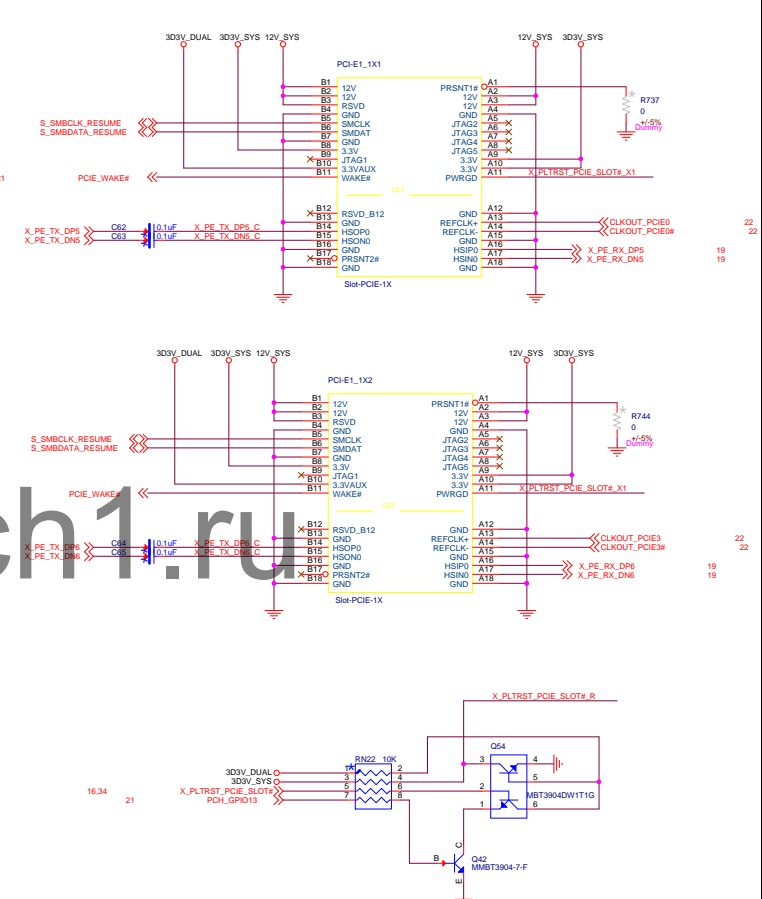
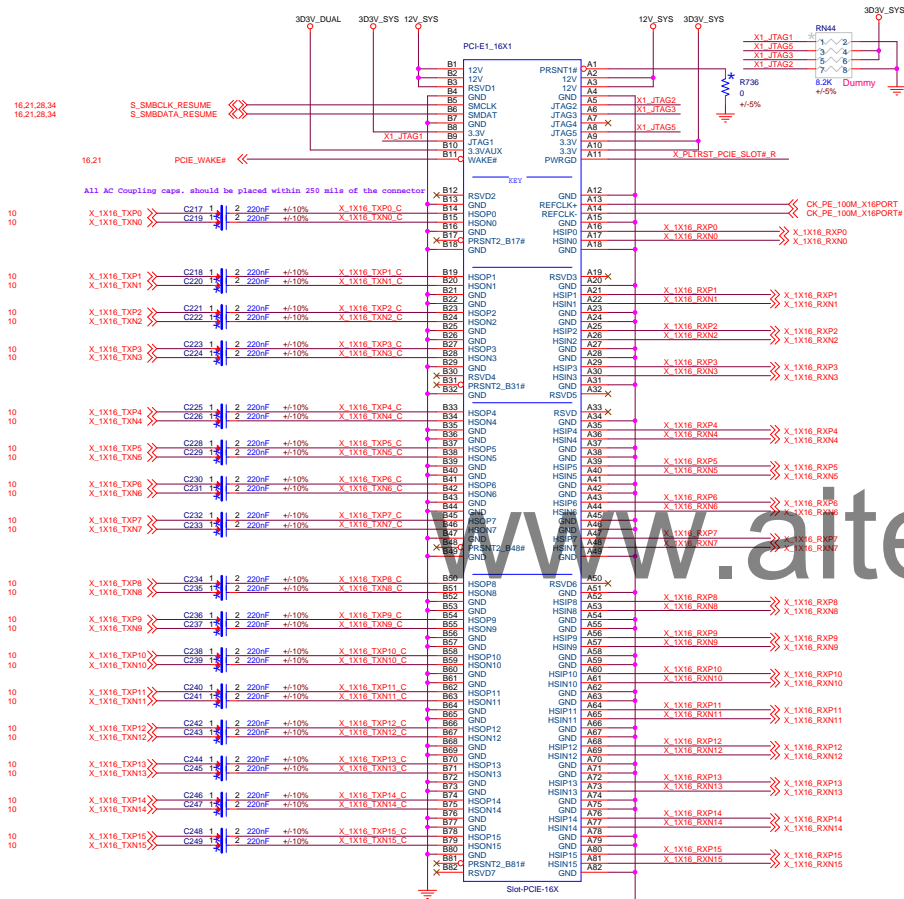


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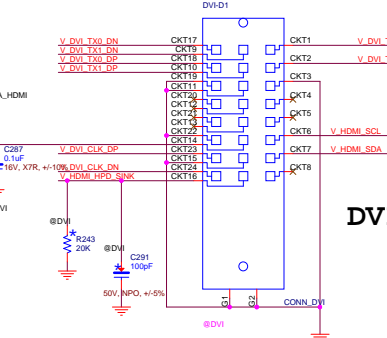
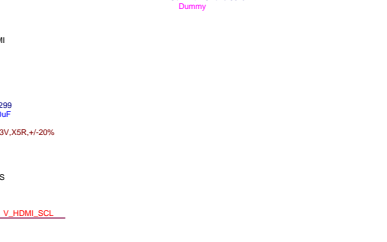
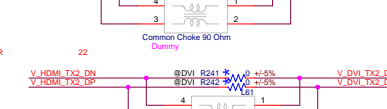
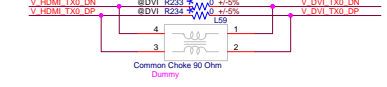
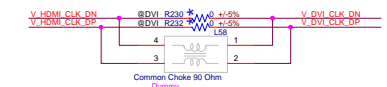
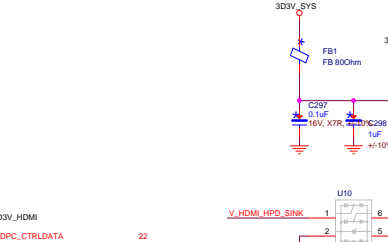
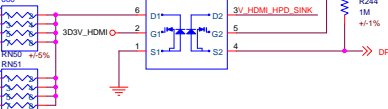
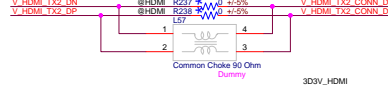
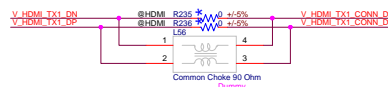
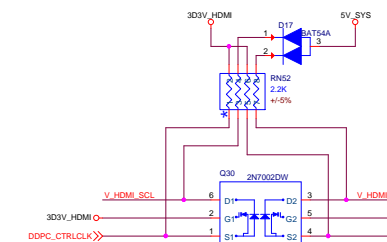
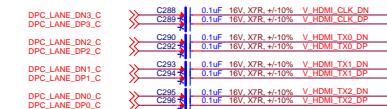
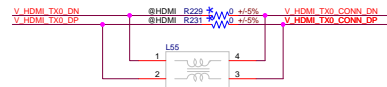
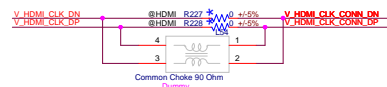
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PCI EXPRESS X1 SLOT1

PCI EXPRESS x16 SLOT

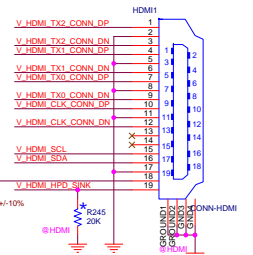


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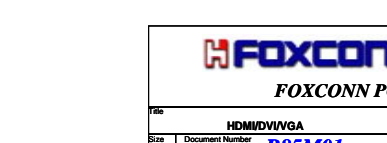
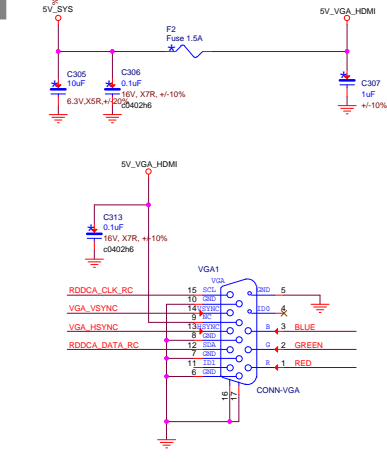
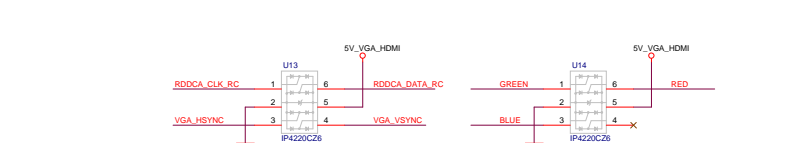
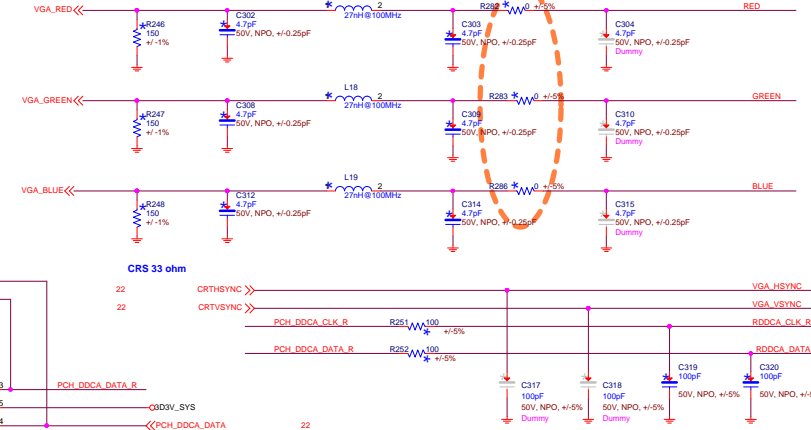
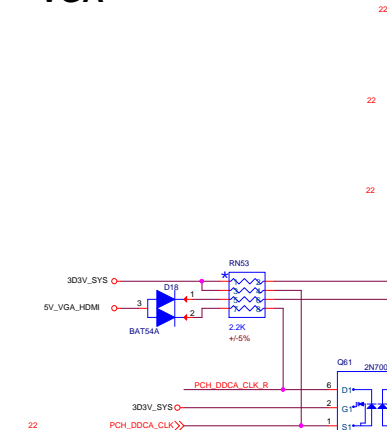


DVI-D

HDMI



VGA

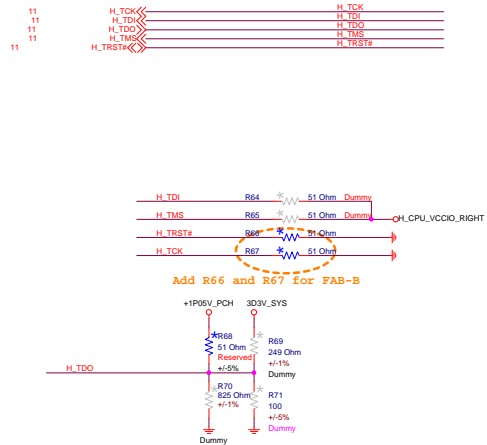


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Intel CPU XDP Debug Connector



Intel PCH XDP Debug Connector

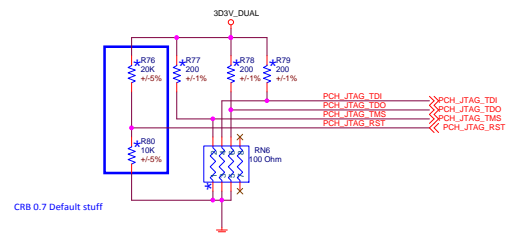


Table 3-1. Processor XDP Connector Pinout

Pin	XDP Signal Name	Target Signal	I/O	Device	Pin	XDP Signal Name	Target Signal	I/O	Device
1	OSDRN_A0	OSDRN_A0	I/O	processor 0	43	OSDRN_C0	CQ[15]	I/O	processor 0
2	OSDRN_A1	OSDRN_A1	I/O	processor 0	44	OSDRN_C1	CQ[16]	I/O	processor 0
3	OSDRN_A2	OSDRN_A2	I/O	processor 0	45	OSDRN_C2	CQ[17]	I/O	processor 0
9	OSDRN_A10	OSDRN_A10	I/O	processor 10	51	OSDRN_C10	CQ[23]	I/O	processor 10
10	OSDRN_A11	OSDRN_A11	I/O	processor 11	52	OSDRN_C11	CQ[24]	I/O	processor 11
11	OSDRN_A12	OSDRN_A12	I/O	processor 12	53	OSDRN_C12	CQ[25]	I/O	processor 12
15	OSDRN_A15	OSDRN_A15	I/O	processor 15	57	OSDRN_C15	CQ[29]	I/O	processor 15
16	OSDRN_A16	OSDRN_A16	I/O	processor 16	58	OSDRN_C16	CQ[30]	I/O	processor 16
19	OSDRN_A19	OSDRN_A19	I/O	processor 19	61	OSDRN_C19	CQ[33]	I/O	processor 19
20	OSDRN_B0	OSDRN_B0	I/O	processor 20	62	OSDRN_C20	CQ[34]	I/O	processor 20
21	OSDRN_B1	OSDRN_B1	I/O	processor 21	63	OSDRN_C21	CQ[35]	I/O	processor 21
24	OSDRN_B4	OSDRN_B4	I/O	processor 24	66	OSDRN_C24	CQ[38]	I/O	processor 24
25	OSDRN_B5	OSDRN_B5	I/O	processor 25	67	OSDRN_C25	CQ[39]	I/O	processor 25
28	OSDRN_B8	OSDRN_B8	I/O	processor 28	70	OSDRN_C28	CQ[42]	I/O	processor 28
29	OSDRN_B9	OSDRN_B9	I/O	processor 29	71	OSDRN_C29	CQ[43]	I/O	processor 29
31	OSDRN_B11	OSDRN_B11	I/O	processor 31	73	OSDRN_C31	CQ[45]	I/O	processor 31
32	OSDRN_B12	OSDRN_B12	I/O	processor 32	74	OSDRN_C32	CQ[46]	I/O	processor 32
33	OSDRN_B13	OSDRN_B13	I/O	processor 33	75	OSDRN_C33	CQ[47]	I/O	processor 33
39	OSDRN_B19	OSDRN_B19	I/O	processor 39	81	OSDRN_C39	CQ[53]	I/O	processor 39
40	OSDRN_B20	OSDRN_B20	I/O	processor 40	82	OSDRN_C40	CQ[54]	I/O	processor 40
41	OSDRN_B21	OSDRN_B21	I/O	processor 41	83	OSDRN_C41	CQ[55]	I/O	processor 41
43	VCC_OSD1	VCC_OSD1	I/O	processor 43	85	OSDRN_C43	CQ[57]	I/O	processor 43
44	VCC_OSD1	VCC_OSD1	I/O	processor 44	86	OSDRN_C44	CQ[58]	I/O	processor 44
45	VCC_OSD1	VCC_OSD1	I/O	processor 45	87	OSDRN_C45	CQ[59]	I/O	processor 45
46	VCC_OSD1	VCC_OSD1	I/O	processor 46	88	OSDRN_C46	CQ[60]	I/O	processor 46
47	VCC_OSD1	VCC_OSD1	I/O	processor 47	89	OSDRN_C47	CQ[61]	I/O	processor 47
48	VCC_OSD1	VCC_OSD1	I/O	processor 48	90	OSDRN_C48	CQ[62]	I/O	processor 48
49	VCC_OSD1	VCC_OSD1	I/O	processor 49	91	OSDRN_C49	CQ[63]	I/O	processor 49
50	VCC_OSD1	VCC_OSD1	I/O	processor 50	92	OSDRN_C50	CQ[64]	I/O	processor 50
51	VCC_OSD1	VCC_OSD1	I/O	processor 51	93	OSDRN_C51	CQ[65]	I/O	processor 51
52	VCC_OSD1	VCC_OSD1	I/O	processor 52	94	OSDRN_C52	CQ[66]	I/O	processor 52
53	VCC_OSD1	VCC_OSD1	I/O	processor 53	95	OSDRN_C53	CQ[67]	I/O	processor 53
54	VCC_OSD1	VCC_OSD1	I/O	processor 54	96	OSDRN_C54	CQ[68]	I/O	processor 54
55	VCC_OSD1	VCC_OSD1	I/O	processor 55	97	OSDRN_C55	CQ[69]	I/O	processor 55
56	VCC_OSD1	VCC_OSD1	I/O	processor 56	98	OSDRN_C56	CQ[70]	I/O	processor 56
57	VCC_OSD1	VCC_OSD1	I/O	processor 57	99	OSDRN_C57	CQ[71]	I/O	processor 57
58	VCC_OSD1	VCC_OSD1	I/O	processor 58	100	OSDRN_C58	CQ[72]	I/O	processor 58
59	VCC_OSD1	VCC_OSD1	I/O	processor 59	101	OSDRN_C59	CQ[73]	I/O	processor 59
60	VCC_OSD1	VCC_OSD1	I/O	processor 60	102	OSDRN_C60	CQ[74]	I/O	processor 60
61	VCC_OSD1	VCC_OSD1	I/O	processor 61	103	OSDRN_C61	CQ[75]	I/O	processor 61
62	VCC_OSD1	VCC_OSD1	I/O	processor 62	104	OSDRN_C62	CQ[76]	I/O	processor 62
63	VCC_OSD1	VCC_OSD1	I/O	processor 63	105	OSDRN_C63	CQ[77]	I/O	processor 63
64	VCC_OSD1	VCC_OSD1	I/O	processor 64	106	OSDRN_C64	CQ[78]	I/O	processor 64
65	VCC_OSD1	VCC_OSD1	I/O	processor 65	107	OSDRN_C65	CQ[79]	I/O	processor 65
66	VCC_OSD1	VCC_OSD1	I/O	processor 66	108	OSDRN_C66	CQ[80]	I/O	processor 66
67	VCC_OSD1	VCC_OSD1	I/O	processor 67	109	OSDRN_C67	CQ[81]	I/O	processor 67
68	VCC_OSD1	VCC_OSD1	I/O	processor 68	110	OSDRN_C68	CQ[82]	I/O	processor 68
69	VCC_OSD1	VCC_OSD1	I/O	processor 69	111	OSDRN_C69	CQ[83]	I/O	processor 69
70	VCC_OSD1	VCC_OSD1	I/O	processor 70	112	OSDRN_C70	CQ[84]	I/O	processor 70
71	VCC_OSD1	VCC_OSD1	I/O	processor 71	113	OSDRN_C71	CQ[85]	I/O	processor 71
72	VCC_OSD1	VCC_OSD1	I/O	processor 72	114	OSDRN_C72	CQ[86]	I/O	processor 72
73	VCC_OSD1	VCC_OSD1	I/O	processor 73	115	OSDRN_C73	CQ[87]	I/O	processor 73
74	VCC_OSD1	VCC_OSD1	I/O	processor 74	116	OSDRN_C74	CQ[88]	I/O	processor 74
75	VCC_OSD1	VCC_OSD1	I/O	processor 75	117	OSDRN_C75	CQ[89]	I/O	processor 75
76	VCC_OSD1	VCC_OSD1	I/O	processor 76	118	OSDRN_C76	CQ[90]	I/O	processor 76
77	VCC_OSD1	VCC_OSD1	I/O	processor 77	119	OSDRN_C77	CQ[91]	I/O	processor 77
78	VCC_OSD1	VCC_OSD1	I/O	processor 78	120	OSDRN_C78	CQ[92]	I/O	processor 78
79	VCC_OSD1	VCC_OSD1	I/O	processor 79	121	OSDRN_C79	CQ[93]	I/O	processor 79
80	VCC_OSD1	VCC_OSD1	I/O	processor 80	122	OSDRN_C80	CQ[94]	I/O	processor 80
81	VCC_OSD1	VCC_OSD1	I/O	processor 81	123	OSDRN_C81	CQ[95]	I/O	processor 81
82	VCC_OSD1	VCC_OSD1	I/O	processor 82	124	OSDRN_C82	CQ[96]	I/O	processor 82
83	VCC_OSD1	VCC_OSD1	I/O	processor 83	125	OSDRN_C83	CQ[97]	I/O	processor 83
84	VCC_OSD1	VCC_OSD1	I/O	processor 84	126	OSDRN_C84	CQ[98]	I/O	processor 84
85	VCC_OSD1	VCC_OSD1	I/O	processor 85	127	OSDRN_C85	CQ[99]	I/O	processor 85
86	VCC_OSD1	VCC_OSD1	I/O	processor 86	128	OSDRN_C86	CQ[100]	I/O	processor 86
87	VCC_OSD1	VCC_OSD1	I/O	processor 87	129	OSDRN_C87	CQ[101]	I/O	processor 87
88	VCC_OSD1	VCC_OSD1	I/O	processor 88	130	OSDRN_C88	CQ[102]	I/O	processor 88
89	VCC_OSD1	VCC_OSD1	I/O	processor 89	131	OSDRN_C89	CQ[103]	I/O	processor 89
90	VCC_OSD1	VCC_OSD1	I/O	processor 90	132	OSDRN_C90	CQ[104]	I/O	processor 90
91	VCC_OSD1	VCC_OSD1	I/O	processor 91	133	OSDRN_C91	CQ[105]	I/O	processor 91
92	VCC_OSD1	VCC_OSD1	I/O	processor 92	134	OSDRN_C92	CQ[106]	I/O	processor 92
93	VCC_OSD1	VCC_OSD1	I/O	processor 93	135	OSDRN_C93	CQ[107]	I/O	processor 93
94	VCC_OSD1	VCC_OSD1	I/O	processor 94	136	OSDRN_C94	CQ[108]	I/O	processor 94
95	VCC_OSD1	VCC_OSD1	I/O	processor 95	137	OSDRN_C95	CQ[109]	I/O	processor 95
96	VCC_OSD1	VCC_OSD1	I/O	processor 96	138	OSDRN_C96	CQ[110]	I/O	processor 96
97	VCC_OSD1	VCC_OSD1	I/O	processor 97	139	OSDRN_C97	CQ[111]	I/O	processor 97
98	VCC_OSD1	VCC_OSD1	I/O	processor 98	140	OSDRN_C98	CQ[112]	I/O	processor 98
99	VCC_OSD1	VCC_OSD1	I/O	processor 99	141	OSDRN_C99	CQ[113]	I/O	processor 99
100	VCC_OSD1	VCC_OSD1	I/O	processor 100	142	OSDRN_C100	CQ[114]	I/O	processor 100
101	VCC_OSD1	VCC_OSD1	I/O	processor 101	143	OSDRN_C101	CQ[115]	I/O	processor 101
102	VCC_OSD1	VCC_OSD1	I/O	processor 102	144	OSDRN_C102	CQ[116]	I/O	processor 102
103	VCC_OSD1	VCC_OSD1	I/O	processor 103	145	OSDRN_C103	CQ[117]	I/O	processor 103
104	VCC_OSD1	VCC_OSD1	I/O	processor 104	146	OSDRN_C104	CQ[118]	I/O	processor 104
105	VCC_OSD1	VCC_OSD1	I/O	processor 105	147	OSDRN_C105	CQ[119]	I/O	processor 105
106	VCC_OSD1	VCC_OSD1	I/O	processor 106	148	OSDRN_C106	CQ[120]	I/O	processor 106
107	VCC_OSD1	VCC_OSD1	I/O	processor 107	149	OSDRN_C107	CQ[121]	I/O	processor 107
108	VCC_OSD1	VCC_OSD1	I/O	processor 108	150	OSDRN_C108	CQ[122]	I/O	processor 108
109	VCC_OSD1	VCC_OSD1	I/O	processor 109	151	OSDRN_C109	CQ[123]	I/O	processor 109
110	VCC_OSD1	VCC_OSD1	I/O	processor 110	152	OSDRN_C110	CQ[124]	I/O	processor 110
111	VCC_OSD1	VCC_OSD1	I/O	processor 111	153	OSDRN_C111	CQ[125]	I/O	processor 111
112	VCC_OSD1	VCC_OSD1	I/O	processor 112	154	OSDRN_C112	CQ[126]	I/O	processor 112
113	VCC_OSD1	VCC_OSD1	I/O	processor 113	155	OSDRN_C113	CQ[127]	I/O	processor 113
114	VCC_OSD1	VCC_OSD1	I/O	processor 114	156	OSDRN_C114	CQ[128]	I/O	processor 114
115	VCC_OSD1	VCC_OSD1	I/O	processor 115	157	OSDRN_C115	CQ[129]	I/O	processor 115
116	VCC_OSD1	VCC_OSD1	I/O	processor 116	158	OSDRN_C116	CQ[130]	I/O	processor 116
117	VCC_OSD1	VCC_OSD1	I/O	processor 117	159	OSDRN_C117	CQ[131]	I/O	processor 117
118	VCC_OSD1	VCC_OSD1	I/O	processor 118	160	OSDRN_C118	CQ[132]	I/O	processor 118
119	VCC_OSD1	VCC_OSD1	I/O	processor 119	161	OSDRN_C119	CQ[133]	I/O	processor 119
120	VCC_OSD1	VCC_OSD1	I/O	processor 120	162	OSDRN_C120	CQ[134]	I/O	processor 120
121	VCC_OSD1	VCC_OSD1	I/O	processor 121	163	OSDRN_C121	CQ[135]	I/O	processor 121
122	VCC_OSD1	VCC_OSD1	I/O	processor 122	164	OSDRN_C122	CQ[136]	I/O	processor 122
123	VCC_OSD1	VCC_OSD1	I/O	processor 123	165	OSDRN_C123	CQ[137]	I/O	processor 123
124	VCC_OSD1	VCC_OSD1	I/O	processor 124	166	OSDRN_C124	CQ[138]	I/O	processor 124
125	VCC_OSD1	VCC_OSD1	I/O	processor 125	167	OSDRN_C125	CQ[139]	I/O	processor 125
126	VCC_OSD1	VCC_OSD1	I/O	processor 126	168	OSDRN_C126	CQ[140]	I/O	processor 126
127	VCC_OSD1	VCC_OSD1	I/O	processor 127	169	OSDRN_C127	CQ[141]	I/O	processor 127
128	VCC_OSD1	VCC_OSD1	I/O	processor 128	170	OSDRN_C128	CQ[142]	I/O	processor 128
129	VCC_OSD1	VCC_OSD1	I/O	processor 129	171	OSDRN_C129	CQ[143]	I/O	processor 129
130	VCC_OSD1	VCC_OSD1	I/O	processor 130	172	OSDRN_C130	CQ[144]	I/O	processor 130
131	VCC_OSD1	VCC_OSD1	I/O	processor 131	173	OSDRN_C131	CQ[145]	I/O	processor 131
132	VCC_OSD1	VCC_OSD1	I/O	processor 132	174	OSDRN_C132	CQ[146]	I/O	processor 132
133	VCC_OSD1	VCC_OSD1	I/O	processor 133	175	OSDRN_C133	CQ[147]	I/O	processor 133
134	VCC_OSD1	VCC_OSD1	I/O	processor 134	176	OSDRN_C134	CQ[148]	I/O	processor 134
135	VCC_OSD1	VCC_OSD1	I/O	processor 135	177	OSDRN_C135	CQ[149]	I/O	processor 135
136	VCC_OSD1	VCC_OSD1	I/O	processor 136	178	OSDRN_C136	CQ[150]	I/O	processor 136
137	VCC_OSD1	VCC_OSD1	I/O	processor 137	179	OSDRN_C137	CQ[151]	I/O	processor 137
138	VCC_OSD1	VCC_OSD1	I/O	processor 138	180	OSDRN_C138	CQ[152]	I/O	processor 138
139	VCC_OSD1	VCC_OSD1	I/O	processor 139	181	OSDRN_C139	CQ[153]	I/O	processor 139
140	VCC_OSD1	VCC_OSD1	I/O	processor 140	182	OSDRN_C140	CQ[154]	I/O	processor 140
141	VCC_OSD1	VCC_OSD1	I/O	processor 141	183	OSDRN_C141	CQ[155]	I/O	processor 141
142	VCC_OSD1	VCC_OSD1	I/O	processor 142	184	OSDRN_C142	CQ[156]	I/O	processor 142
143	VCC_OSD1	VCC_OSD1	I/O	processor 143	185	OSDRN_C143	CQ[157]	I/O	processor 143
144	VCC_OSD1	VCC_OSD1	I/O	processor 144	186	OSDRN_C144	CQ[158]	I/O	processor 144
145	VCC_OSD1	VCC_OSD1	I/O	processor 145	187	OSDRN_C145	CQ[159]	I/O	processor 145
146	VCC_OSD1	VCC_OSD1	I/O	processor 146	188	OSDRN_C146	CQ[160]	I/O	processor 146
147	VCC_OSD1	VCC_OSD1	I/O	processor 147	189	OSDRN_C147	CQ[161]	I/O	processor 147
148	VCC_OSD1	VCC_OSD1	I/O	processor 148	190	OSDRN_C148	CQ[162]	I/O	processor 148
149	VCC_OSD1	VCC_OSD1	I/O	processor 149	191	OSDRN_C149	CQ[163]	I/O	processor 149
150	VCC_OSD1	VCC_OSD1	I/O	processor 150	192	OSDRN_C150	CQ[164]	I/O	processor 150
151	VCC_OSD1	VCC_OSD1	I/O	processor 151	193	OSDRN_C151	CQ[165]	I/O	processor 151
152	VCC_OSD1	VCC_OSD1	I/O	processor 152	194	OSDRN_C152	CQ[166]	I/O	processor 152
153	VCC_OSD1	VCC_OSD1	I/O	processor 153	195	OSDRN_C153	CQ[167]	I/O	processor 153
154	VCC_OSD1	VCC_OSD1	I/O	processor 154	196	OSDRN_C154	CQ[168]	I/O	processor 154
155	VCC_OSD1	VCC_OSD1	I/O	processor 155	197	OSDRN_C155	CQ[169]	I/O	processor 155
156	VCC_OSD1	VCC_OSD1	I/O	processor 156	198	OSDRN_C156	CQ[170]	I/O	processor 156
157	VCC_OSD1	VCC_OSD1	I/O	processor 157	199	OSDRN_C157	CQ[171]	I/O	processor 157
158	VCC_OSD1	VCC_OSD1	I/O	processor 158	200	OSDRN_C158	CQ[172]	I/O	processor 158
159	VCC_OSD1	VCC_OSD1	I/O	processor 159	201	OSDRN_C159	CQ		

Intel DMI LAI Footprint

This is footprint only . BOM is Dummy

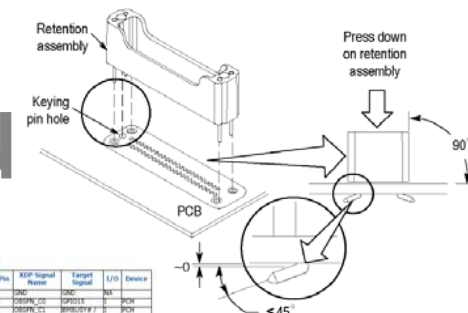
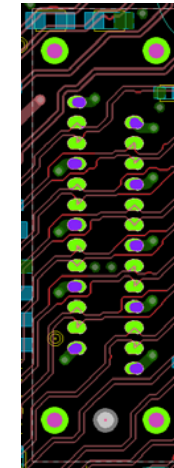


Table 4-1. PCH XDP Connector Pinout

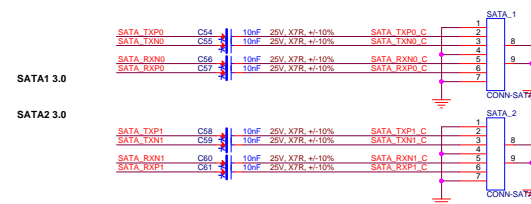
Pin	XDP Signal Name	Target Signal	I/O	Device	Pin	XDP Signal Name	Target Signal	I/O	Device
1	DSPPA_A1	DSPPA	AN	8	DSPPA_C1	DSPPA	AN	8	DSPPA_C1
2	DSPPA_B1	DSPPA	AN	8	DSPPA_C2	DSPPA	AN	8	DSPPA_C2
3	DSPPA_C1	DSPPA	AN	8	DSPPA_C3	DSPPA	AN	8	DSPPA_C3
4	DSPPA_C2	DSPPA	AN	8	DSPPA_C4	DSPPA	AN	8	DSPPA_C4
5	DSPPA_C3	DSPPA	AN	8	DSPPA_C5	DSPPA	AN	8	DSPPA_C5
6	DSPPA_C4	DSPPA	AN	8	DSPPA_C6	DSPPA	AN	8	DSPPA_C6
7	DSPPA_C5	DSPPA	AN	8	DSPPA_C7	DSPPA	AN	8	DSPPA_C7
8	DSPPA_C6	DSPPA	AN	8	DSPPA_C8	DSPPA	AN	8	DSPPA_C8
9	DSPPA_C7	DSPPA	AN	8	DSPPA_C9	DSPPA	AN	8	DSPPA_C9
10	DSPPA_C8	DSPPA	AN	8	DSPPA_C10	DSPPA	AN	8	DSPPA_C10
11	DSPPA_C9	DSPPA	AN	8	DSPPA_C11	DSPPA	AN	8	DSPPA_C11
12	DSPPA_C10	DSPPA	AN	8	DSPPA_C12	DSPPA	AN	8	DSPPA_C12
13	DSPPA_C11	DSPPA	AN	8	DSPPA_C13	DSPPA	AN	8	DSPPA_C13
14	DSPPA_C12	DSPPA	AN	8	DSPPA_C14	DSPPA	AN	8	DSPPA_C14
15	DSPPA_C13	DSPPA	AN	8	DSPPA_C15	DSPPA	AN	8	DSPPA_C15
16	DSPPA_C14	DSPPA	AN	8	DSPPA_C16	DSPPA	AN	8	DSPPA_C16
17	DSPPA_C15	DSPPA	AN	8	DSPPA_C17	DSPPA	AN	8	DSPPA_C17
18	DSPPA_C16	DSPPA	AN	8	DSPPA_C18	DSPPA	AN	8	DSPPA_C18
19	DSPPA_C17	DSPPA	AN	8	DSPPA_C19	DSPPA	AN	8	DSPPA_C19
20	DSPPA_C18	DSPPA	AN	8	DSPPA_C20	DSPPA	AN	8	DSPPA_C20
21	DSPPA_C19	DSPPA	AN	8	DSPPA_C21	DSPPA	AN	8	DSPPA_C21
22	DSPPA_C20	DSPPA	AN	8	DSPPA_C22	DSPPA	AN	8	DSPPA_C22
23	DSPPA_C21	DSPPA	AN	8	DSPPA_C23	DSPPA	AN	8	DSPPA_C23
24	DSPPA_C22	DSPPA	AN	8	DSPPA_C24	DSPPA	AN	8	DSPPA_C24
25	DSPPA_C23	DSPPA	AN	8	DSPPA_C25	DSPPA	AN	8	DSPPA_C25
26	DSPPA_C24	DSPPA	AN	8	DSPPA_C26	DSPPA	AN	8	DSPPA_C26
27	DSPPA_C25	DSPPA	AN	8	DSPPA_C27	DSPPA	AN	8	DSPPA_C27
28	DSPPA_C26	DSPPA	AN	8	DSPPA_C28	DSPPA	AN	8	DSPPA_C28
29	DSPPA_C27	DSPPA	AN	8	DSPPA_C29	DSPPA	AN	8	DSPPA_C29
30	DSPPA_C28	DSPPA	AN	8	DSPPA_C30	DSPPA	AN	8	DSPPA_C30
31	DSPPA_C29	DSPPA	AN	8	DSPPA_C31	DSPPA	AN	8	DSPPA_C31
32	DSPPA_C30	DSPPA	AN	8	DSPPA_C32	DSPPA	AN	8	DSPPA_C32
33	DSPPA_C31	DSPPA	AN	8	DSPPA_C33	DSPPA	AN	8	DSPPA_C33
34	DSPPA_C32	DSPPA	AN	8	DSPPA_C34	DSPPA	AN	8	DSPPA_C34
35	DSPPA_C33	DSPPA	AN	8	DSPPA_C35	DSPPA	AN	8	DSPPA_C35
36	DSPPA_C34	DSPPA	AN	8	DSPPA_C36	DSPPA	AN	8	DSPPA_C36
37	DSPPA_C35	DSPPA	AN	8	DSPPA_C37	DSPPA	AN	8	DSPPA_C37
38	DSPPA_C36	DSPPA	AN	8	DSPPA_C38	DSPPA	AN	8	DSPPA_C38
39	DSPPA_C37	DSPPA	AN	8	DSPPA_C39	DSPPA	AN	8	DSPPA_C39
40	DSPPA_C38	DSPPA	AN	8	DSPPA_C40	DSPPA	AN	8	DSPPA_C40
41	DSPPA_C39	DSPPA	AN	8	DSPPA_C41	DSPPA	AN	8	DSPPA_C41
42	DSPPA_C40	DSPPA	AN	8	DSPPA_C42	DSPPA	AN	8	DSPPA_C42
43	DSPPA_C41	DSPPA	AN	8	DSPPA_C43	DSPPA	AN	8	DSPPA_C43
44	DSPPA_C42	DSPPA	AN	8	DSPPA_C44	DSPPA	AN	8	DSPPA_C44
45	DSPPA_C43	DSPPA	AN	8	DSPPA_C45	DSPPA	AN	8	DSPPA_C45
46	DSPPA_C44	DSPPA	AN	8	DSPPA_C46	DSPPA	AN	8	DSPPA_C46
47	DSPPA_C45	DSPPA	AN	8	DSPPA_C47	DSPPA	AN	8	DSPPA_C47
48	DSPPA_C46	DSPPA	AN	8	DSPPA_C48	DSPPA	AN	8	DSPPA_C48
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50	DSPPA_C48	DSPPA	AN	8	DSPPA_C50	DSPPA	AN	8	DSPPA_C50
51	DSPPA_C49	DSPPA	AN	8	DSPPA_C51	DSPPA	AN	8	DSPPA_C51
52	DSPPA_C50	DSPPA	AN	8	DSPPA_C52	DSPPA	AN	8	DSPPA_C52
53	DSPPA_C51	DSPPA	AN	8	DSPPA_C53	DSPPA	AN	8	DSPPA_C53
54	DSPPA_C52	DSPPA	AN	8	DSPPA_C54	DSPPA	AN	8	DSPPA_C54
55	DSPPA_C53	DSPPA	AN	8	DSPPA_C55	DSPPA	AN	8	DSPPA_C55
56	DSPPA_C54	DSPPA	AN	8	DSPPA_C56	DSPPA	AN	8	DSPPA_C56
57	DSPPA_C55	DSPPA	AN	8	DSPPA_C57	DSPPA	AN	8	DSPPA_C57
58	DSPPA_C56	DSPPA	AN	8	DSPPA_C58	DSPPA	AN	8	DSPPA_C58
59	DSPPA_C57	DSPPA	AN	8	DSPPA_C59	DSPPA	AN	8	DSPPA_C59
60	DSPPA_C58	DSPPA	AN	8	DSPPA_C60	DSPPA	AN	8	DSPPA_C60
61	DSPPA_C59	DSPPA	AN	8	DSPPA_C61	DSPPA	AN	8	DSPPA_C61
62	DSPPA_C60	DSPPA	AN	8	DSPPA_C62	DSPPA	AN	8	DSPPA_C62
63	DSPPA_C61	DSPPA	AN	8	DSPPA_C63	DSPPA	AN	8	DSPPA_C63
64	DSPPA_C62	DSPPA	AN	8	DSPPA_C64	DSPPA	AN	8	DSPPA_C64
65	DSPPA_C63	DSPPA	AN	8	DSPPA_C65	DSPPA	AN	8	DSPPA_C65
66	DSPPA_C64	DSPPA	AN	8	DSPPA_C66	DSPPA	AN	8	DSPPA_C66
67	DSPPA_C65	DSPPA	AN	8	DSPPA_C67	DSPPA	AN	8	DSPPA_C67
68	DSPPA_C66	DSPPA	AN	8	DSPPA_C68	DSPPA	AN	8	DSPPA_C68
69	DSPPA_C67	DSPPA	AN	8	DSPPA_C69	DSPPA	AN	8	DSPPA_C69
70	DSPPA_C68	DSPPA	AN	8	DSPPA_C70	DSPPA	AN	8	DSPPA_C70
71	DSPPA_C69	DSPPA	AN	8	DSPPA_C71	DSPPA	AN	8	DSPPA_C71
72	DSPPA_C70	DSPPA	AN	8	DSPPA_C72	DSPPA	AN	8	DSPPA_C72
73	DSPPA_C71	DSPPA	AN	8	DSPPA_C73	DSPPA	AN	8	DSPPA_C73
74	DSPPA_C72	DSPPA	AN	8	DSPPA_C74	DSPPA	AN	8	DSPPA_C74
75	DSPPA_C73	DSPPA	AN	8	DSPPA_C75	DSPPA	AN	8	DSPPA_C75
76	DSPPA_C74	DSPPA	AN	8	DSPPA_C76	DSPPA	AN	8	DSPPA_C76
77	DSPPA_C75	DSPPA	AN	8	DSPPA_C77	DSPPA	AN	8	DSPPA_C77
78	DSPPA_C76	DSPPA	AN	8	DSPPA_C78	DSPPA	AN	8	DSPPA_C78
79	DSPPA_C77	DSPPA	AN	8	DSPPA_C79	DSPPA	AN	8	DSPPA_C79
80	DSPPA_C78	DSPPA	AN	8	DSPPA_C80	DSPPA	AN	8	DSPPA_C80
81	DSPPA_C79	DSPPA	AN	8	DSPPA_C81	DSPPA	AN	8	DSPPA_C81
82	DSPPA_C80	DSPPA	AN	8	DSPPA_C82	DSPPA	AN	8	DSPPA_C82
83	DSPPA_C81	DSPPA	AN	8	DSPPA_C83	DSPPA	AN	8	DSPPA_C83
84	DSPPA_C82	DSPPA	AN	8	DSPPA_C84	DSPPA	AN	8	DSPPA_C84
85	DSPPA_C83	DSPPA	AN	8	DSPPA_C85	DSPPA	AN	8	DSPPA_C85
86	DSPPA_C84	DSPPA	AN	8	DSPPA_C86	DSPPA	AN	8	DSPPA_C86
87	DSPPA_C85	DSPPA	AN	8	DSPPA_C87	DSPPA	AN	8	DSPPA_C87
88	DSPPA_C86	DSPPA	AN	8	DSPPA_C88	DSPPA	AN	8	DSPPA_C88
89	DSPPA_C87	DSPPA	AN	8	DSPPA_C89	DSPPA	AN	8	DSPPA_C89
90	DSPPA_C88	DSPPA	AN	8	DSPPA_C90	DSPPA	AN	8	DSPPA_C90
91	DSPPA_C89	DSPPA	AN	8	DSPPA_C91	DSPPA	AN	8	DSPPA_C91
92	DSPPA_C90	DSPPA	AN	8	DSPPA_C92	DSPPA	AN	8	DSPPA_C92
93	DSPPA_C91	DSPPA	AN	8	DSPPA_C93	DSPPA	AN	8	DSPPA_C93
94	DSPPA_C92	DSPPA	AN	8	DSPPA_C94	DSPPA	AN	8	DSPPA_C94
95	DSPPA_C93	DSPPA	AN	8	DSPPA_C95	DSPPA	AN	8	DSPPA_C95
96	DSPPA_C94	DSPPA	AN	8	DSPPA_C96	DSPPA	AN	8	DSPPA_C96
97	DSPPA_C95	DSPPA	AN	8	DSPPA_C97	DSPPA	AN	8	DSPPA_C97
98	DSPPA_C96	DSPPA	AN	8	DSPPA_C98	DSPPA	AN	8	DSPPA_C98
99	DSPPA_C97	DSPPA	AN	8	DSPPA_C99	DSPPA	AN	8	DSPPA_C99
100	DSPPA_C98	DSPPA	AN	8	DSPPA_C100	DSPPA	AN	8	DSPPA_C100

Change for FAB-B

Change for FAB-B







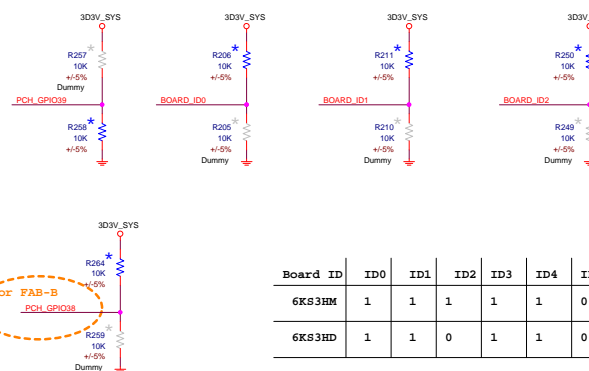
SATA 3.0

Signal	Pin	Value	Signal	Pin	Value
SATA_RX2P	C70	10 μ F 25V X7R, \pm 10%	SATA_TX2P_C	F72	2
SATA_TX2P	C71	10 μ F 25V X7R, \pm 10%	SATA_TX2N_C	F73	2
SATA_RX2N	C72	10 μ F 25V X7R, \pm 10%	SATA_RX2N_C	F74	2
SATA_RX2P2	C73	10 μ F 25V X7R, \pm 10%	SATA_RX2P2_C	F75	2
				F76	7

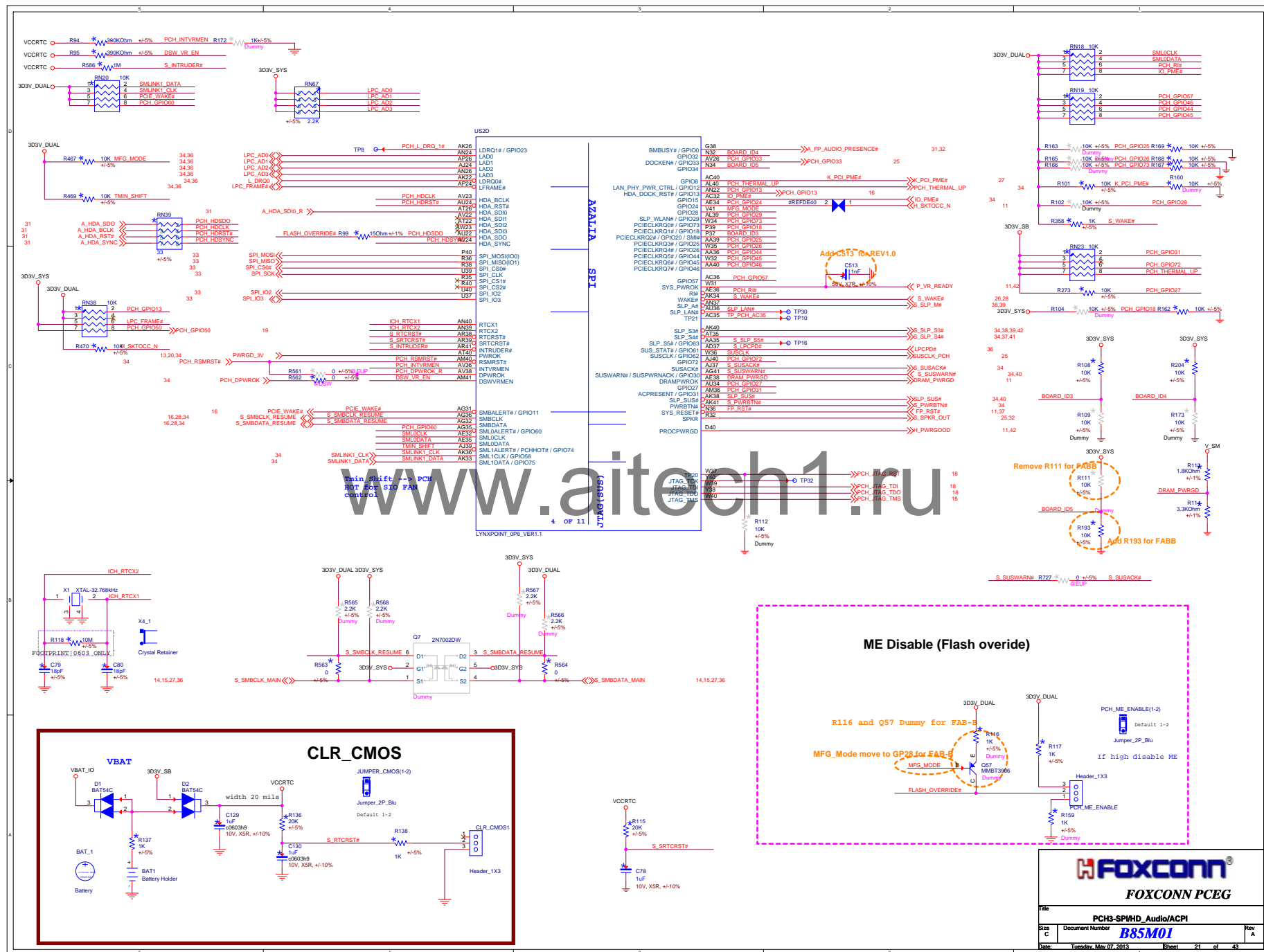
SATA 4.0

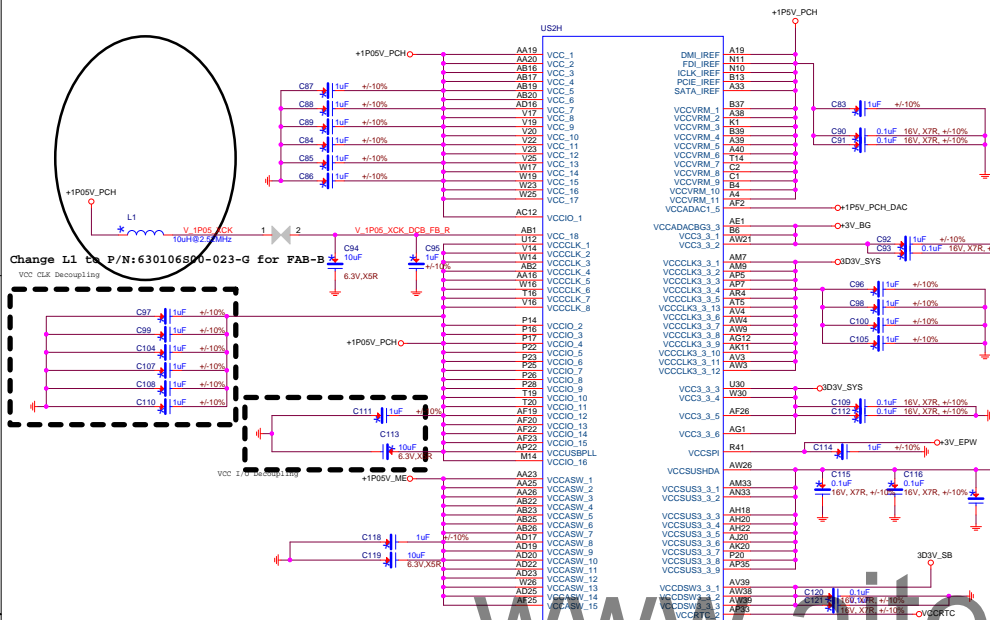
Signal	Pin	Value	Signal	Pin	Value
SATA_RX3P	C74	10 μ F 25V X7R, \pm 10%	SATA_TX3P_C	F77	2
SATA_TX3P	C75	10 μ F 25V X7R, \pm 10%	SATA_TX3N_C	F78	2
SATA_RX3N	C76	10 μ F 25V X7R, \pm 10%	SATA_RX3N_C	F79	2
SATA_RX3P3	C77	10 μ F 25V X7R, \pm 10%	SATA_RX3P3_C	F80	2
				F81	6

CONN-SA



Board ID	ID0	ID1	ID2	ID3	ID4	ID5
6KS3HM	1	1	1	1	1	0
6KS3HD	1	1	0	1	1	0





Filter Requirements for PCH					
Supply	Value	Quantity	Type (Pin Type)	Notes	Placement
VccADAC (pin AF2) Note 1, 2	FB	1	Series Inductor 0603	Rated at least 100 mA	
	0.01uF	1	Filter Capacitor	5%	
	1-Ohm	1	Series Resistor 0402	5%	
VccANCK (pin AB1) Note 2	10uH	1	Series Inductor 0805	Rated at least 100 mA	
	10uF	1	Filter Capacitor	5%	
	0-Ohm	1	Series Resistor 0402	5%	
VccACLK (pin T14) Note 3	10uH	1	Series Inductor 0805	Rated at least 100 mA	
	10uF	1	Filter Capacitor	5%	
	1-Ohm	1	Series Resistor 0402	5%	
VccAFDPLL (pin X1) Note 3	1uH	1	Series Inductor 1210	Rated at least 100 mA	<100 mils (2.54 mm) from PCH
	10uF	1	Filter Capacitor	5%	
	1-Ohm	1	Series Resistor 0402	5%	
VccADMPPLL (pin B37) Note 3	1uH	1	Series Inductor 0805	Rated at least 100 mA	
	10uF	1	Filter Capacitor	5%	
	1-Ohm	1	Series Resistor 0402	5%	
VccADSBPLL (pin C2) Note 3	1uH	1	Series Inductor 0805	Rated at least 100 mA	
	10uF	1	Filter Capacitor	5%	
	1-Ohm	1	Series Resistor 0402	5%	
VccASATAPLL (pin B39) Note 3	10uH	1	Series Inductor 0805	Rated at least 100 mA	
	10uF	1	Filter Capacitor	5%	
	1-Ohm	1	Series Resistor 0402	5%	

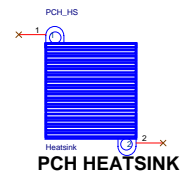


Table 33-2. Decoupling and Power Connection Requirements for PCH (Sheet 1 of 2)

Interface	Voltage Level (V)	VR Rail Name from Figure 31-1, "Platform Power Delivery Map" on page 355	PCH Voltage Rail Name	Place cap(s) near ball(s)	Value	Size	QTY	Placement type: (R)onway, (E)dge, (B)ack
HVCM05	3.3	V3.3 ₅₀	VccSUS3_3	AG1	0.1uF	0402	1	R
PCIe/DME/USB3/SATA	1.05	V1.05 ₅₀	VccIO	P14, P16, P17, P18, P19, M14	10uF	0805	2	R
ACALM	3.3/1.5	V3.3 ₅₀	VccSUS3_3	AW36	0.1uF	0402	1	R
USB2	1.05	V1.05 ₅₀	VccIO	AP22, AF19	1uF	0402	2	E
USB3	3.3	V3.3 ₅₀	Vcc3_3	AW31	1uF	0402	1	E
USB2	3.3	V3.3 ₅₀	VccSUS3_3	AK20	1uF	0402	1	R

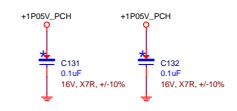
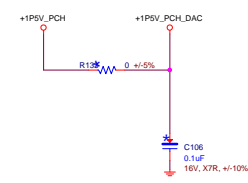
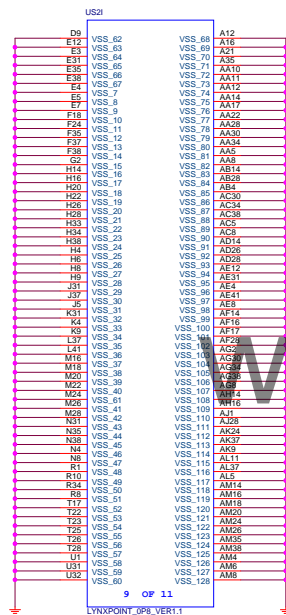


Table 33-2. Decoupling and Power Connection Requirements for PCH (Sheet 2 of 2)

Interface	Voltage Level (V)	VR Rail Name from Figure 31-1, "Platform Power Delivery Map" on page 355	PCH Voltage Rail Name	Place cap(s) near ball(s)	Value	Size	QTY	Placement type: (R)onway, (E)dge, (B)ack
GPIO/LPC/USB3	3.3	V3.3 ₅₀	VccSUS3_3	AN33	0.1uF	0402	1	R
GPIO/LPC	3.3	V3.3 ₅₀	VccDSW3_3	AW39	0.1uF	0402	1	E
GPIO/LPC	-	PCH Internal VRM	DcpSST	AM28	0.1uF	0402	1	E
GPIO/LPC	3.3	V3.3 ₅₀	VccCore3_3	W30	0.1uF	0402	1	R
GPIO/LPC	1.05	V1.05 ₅₀	DcpSustByP	AU40	1uF	0402	1	R
RTC	coin bat	V3.3RTC	VccRTC	AP33	1uF	0402	1	R
RTC	-	PCH Internal VRM	DcpRTC	AW35	0.1uF	0402	1	R
RTC	3.3	V3.3 ₅₀	VccRTC	AP35	1uF	0402	1	R
CPU	1.0/1.05	VCCIO	Vcc_PROC_1 p0	C39	1uF	0603	1	E
SPI	3.3	V3.3 ₅₀	VccSPI	R41	1uF	0402	1	E
Fuse	3.3	V3.3 ₅₀	Vcc3_3	AF36	1uF	0402	1	E
CORE	1.05	VCCIO_MEH	VccASW	AD17, AD19	1uF	0402	1	E
Clock integration	3.3	V3.3 ₅₀	VccCLK3_3	AV4, AR4, AT5, AP5	1uF	0402	4	R
	1.05	V1.05 ₅₀	VccCLK	U12, W14, AB2, AA16, V16, W16	1uF	0402	6	R
Thermal	3.3	V3.3 ₅₀	Vcc3_3	B6	0.1uF	0402	1	E
Core (Note 1)	-	PCH External VRM	DcpSust	AE30, P19, AJ22	1uF	0402	3	E

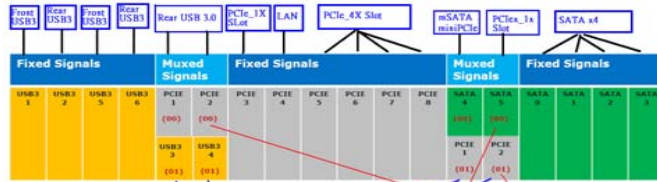


File		
PCH5-PWR		
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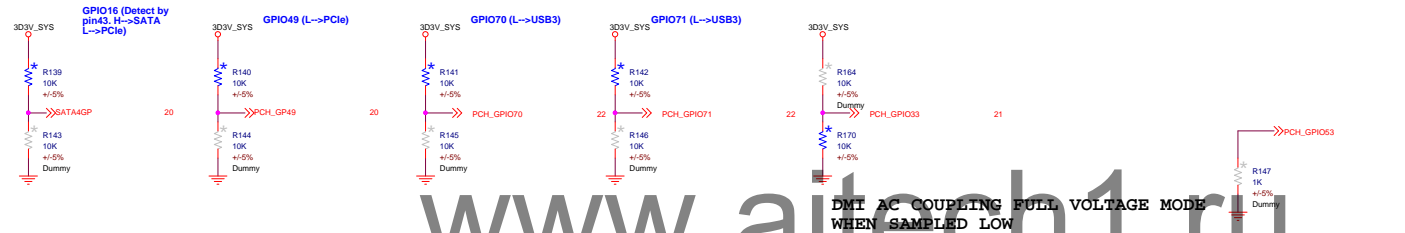


Lynx Point I/O Flexibility

- New architecture allows some I/O Ports to be configured at time of system design



- I/O Flexibility is configured via soft strap
- 00b or 01b: Assign muxed signal to desired port
10b: Reserved
11b: Assign desired port based on GPIO
- Example of soft strap settings



No Reboot Mode

SPER (IN-PD)	Description
High	No reboot mode: Enable
Low	No reboot mode: Disable



TLS Confidentiality

GPIO37 (IN-PD)	Description
High	ME Crypto TLS cipher suite with confidentiality
Low	ME Crypto TLS cipher suite with no confidentiality



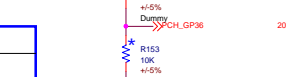
Topblock Swap Mode

GPIO55 (IN-PD)	Description
High	Topblock swap mode: Disable
Low	Topblock swap mode: Enable



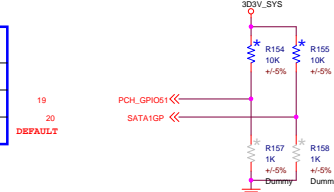
DMI Rx Termination

GPIO36 (IN-PD)	Description
Low	DMI Rx Termination Voltage



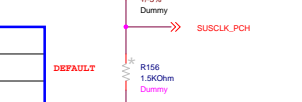
Boot BIOS Destination Selection

GPIO51 (IN-PD)	SATA1GP/GP19 (IN-PD)	Description
Low	Low	Flash cycle routed to LPC
High	Low	Flash cycle routed to PCI
High	High	Flash cycle routed to SPI

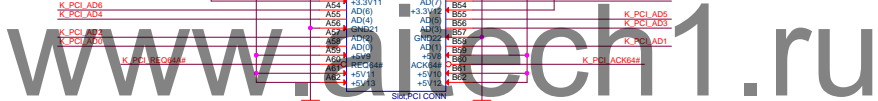


On-Die PLL Voltage Regulator

GPIO62/SUSCLK (IN-PD)	Description
High	Regulator is enabled.
Low	Regulator is disabled.



PCI 1



```

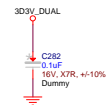
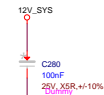
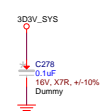
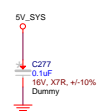
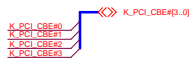
IRQ:  A B C D
IDSEL: AD16
REQ/GNT: 0

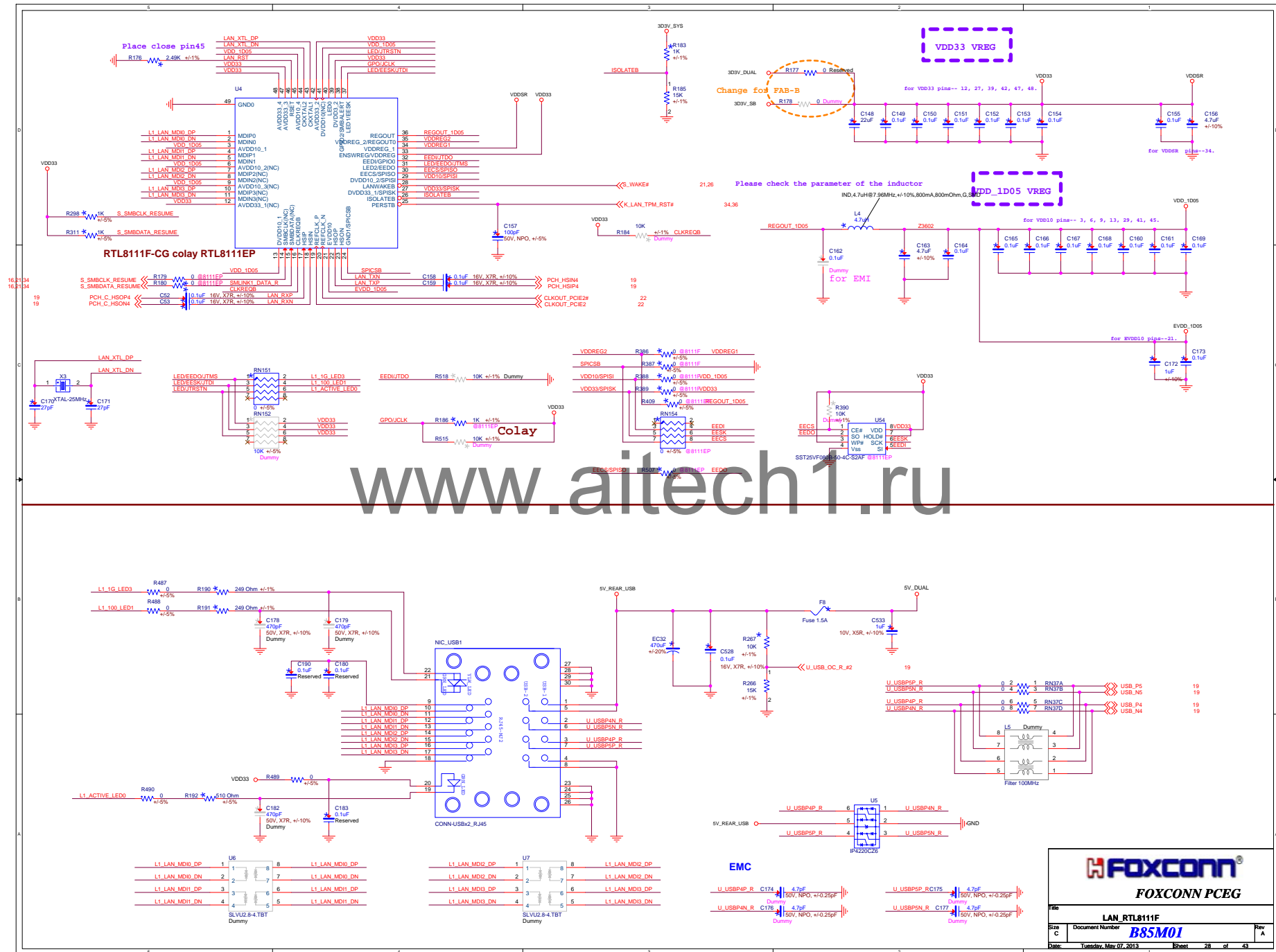
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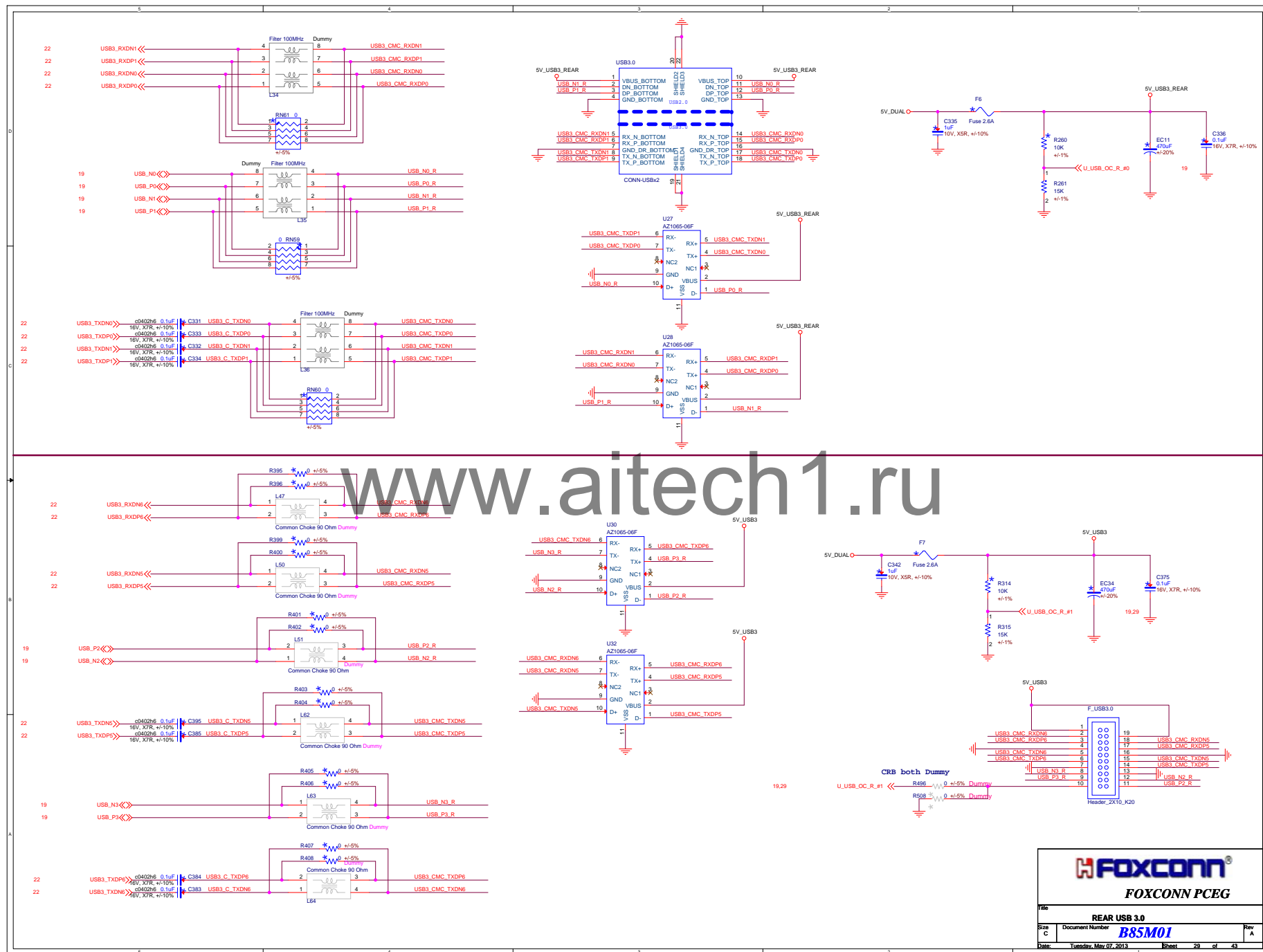
PCI BUS if use 5V external pull up resistor is 2.7K



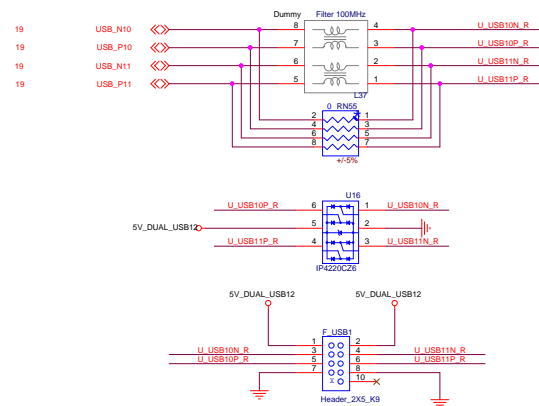
2010.6.22 update



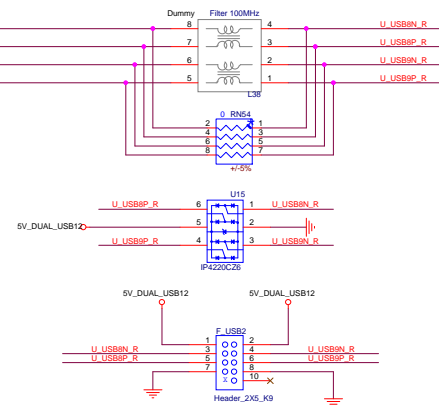




Front_USB1

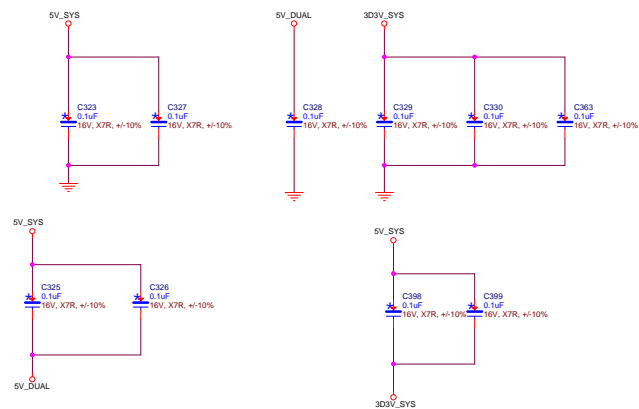
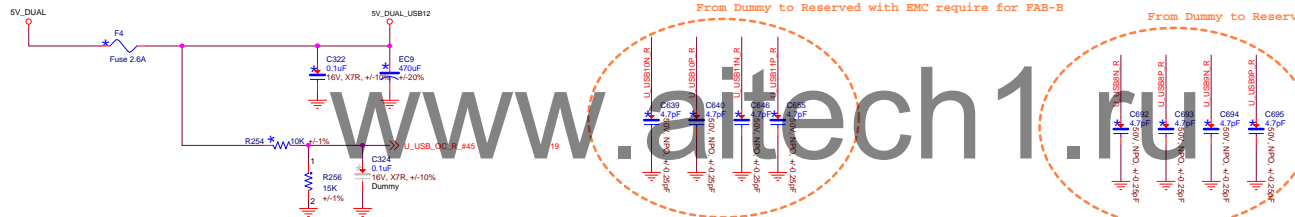


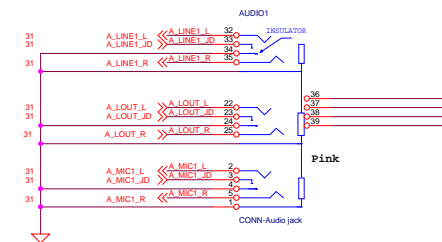
Front_USB2



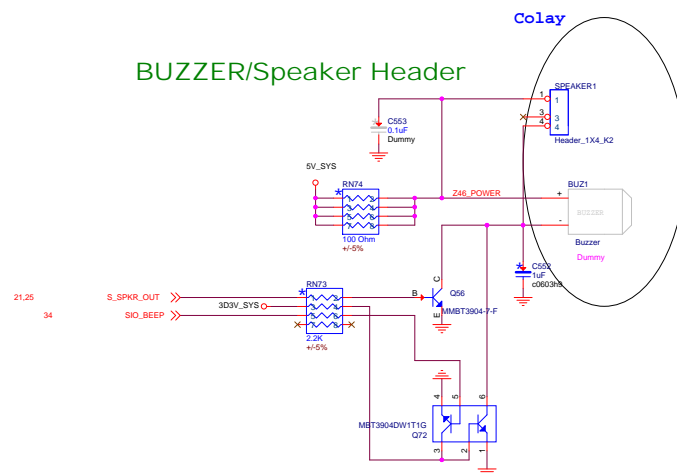
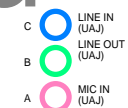
From Dummy to Reserved with EMC require for FAB-B

From Dummy to Reserved with EMC require for FAB-B





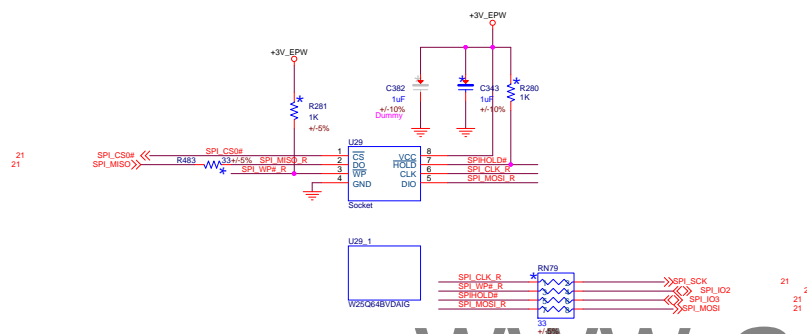
Audio Jack



SPI SOCKET Primary

Place close to SPI ROM

Place close to SPI ROM



Support Quad Read I/O Rom parts. (Beaware of 2nd source need to be support Quad I/O read)

SPI ROMs (move to BOM DIP for factory process)

3. PIN CONFIGURATION SOIC 150 / 208-MIL

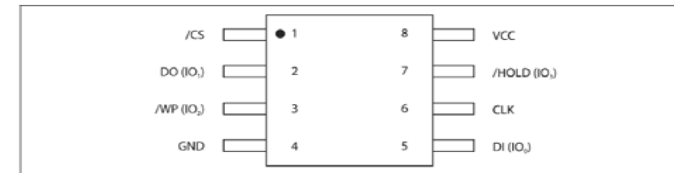


Figure 1a. W25Q16CV Pin Assignments, 8-pin SOIC 150 / 208-mil (Package Code SN & SS)

PIN DESCRIPTION SOIC 150/208-MIL, PDIP 300-MIL AND WSON 6X5-MM

PIN NO.	PIN NAME	I/O	FUNCTION
1	/CS	I	Chip Select Input
2	DO (IO1)	I/O	Data Output (Data Input Output 1)* ¹
3	/WP (IO2)	I/O	Write Protect Input (Data Input Output 2)* ²
4	GND		Ground
5	DI (IO0)	I/O	Data Input (Data Input Output 0)* ¹
6	CLK	I	Serial Clock Input
7	/HOLD (IO3)	I/O	Hold Input (Data Input Output 3)* ²
8	VCC		Power Supply

*1 IO0 and IO1 are used for Standard and Dual SPI instructions

*2 IO0 – IO3 are used for Quad SPI instructions

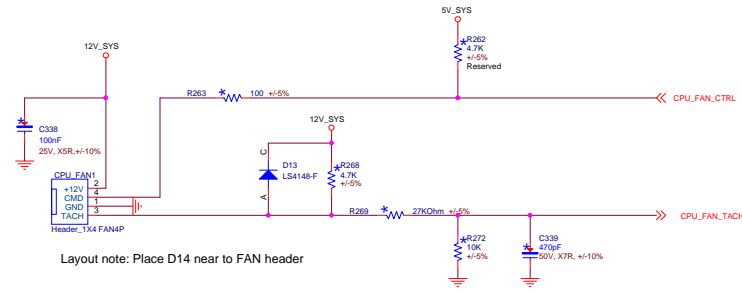


FOXCONN PCEG

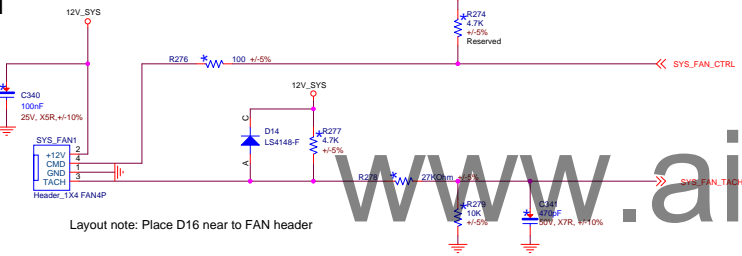
SPI Socket_ROM		
Size C	Document Number B85M01	Rev A
Date: Tuesday, May 07, 2013	Sheet 33 of 43	



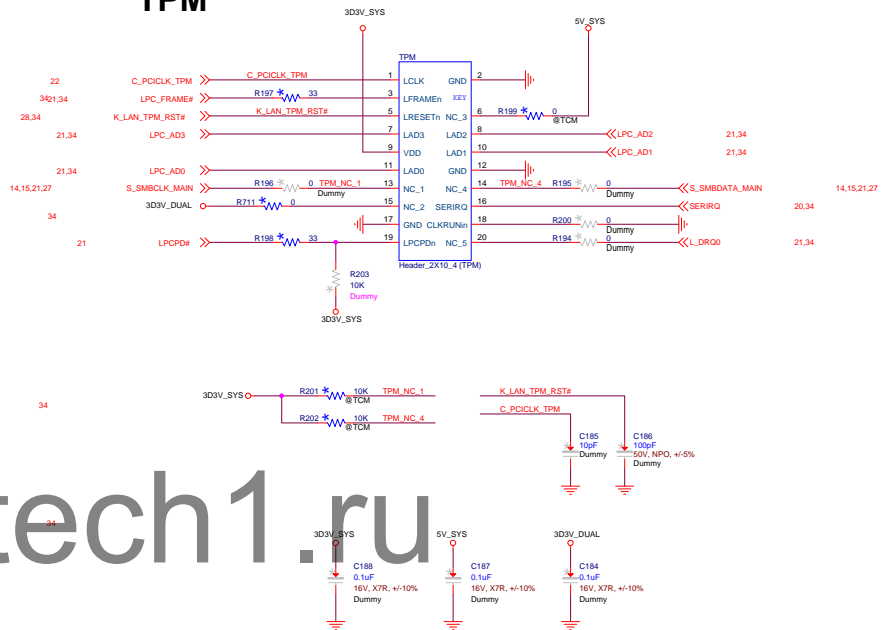
CPU FAN



SYS FAN



TPM

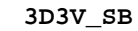


FOXCONN PCEG

FAN Connector		
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	SM_SIOJ	ATXPWRGD	5V_DUAL	5V_S3_N	5V_S3_P
S0	H	H	H	H	H
S4,S5	H	L	L	L	H
S3	L	L	H	L	L

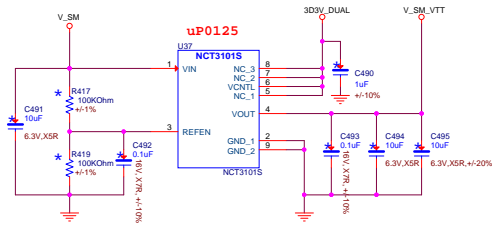
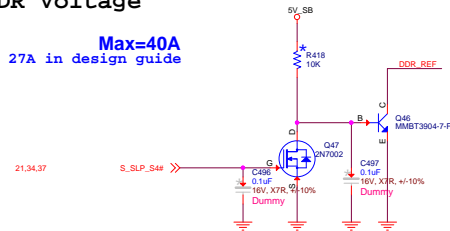


$V_{out} = V_{ref} (1 + R_2/R_1) + I_{adj} R_2$
 $I_{adj} = 50\mu A$
 $V_{ref} = 1.25V$

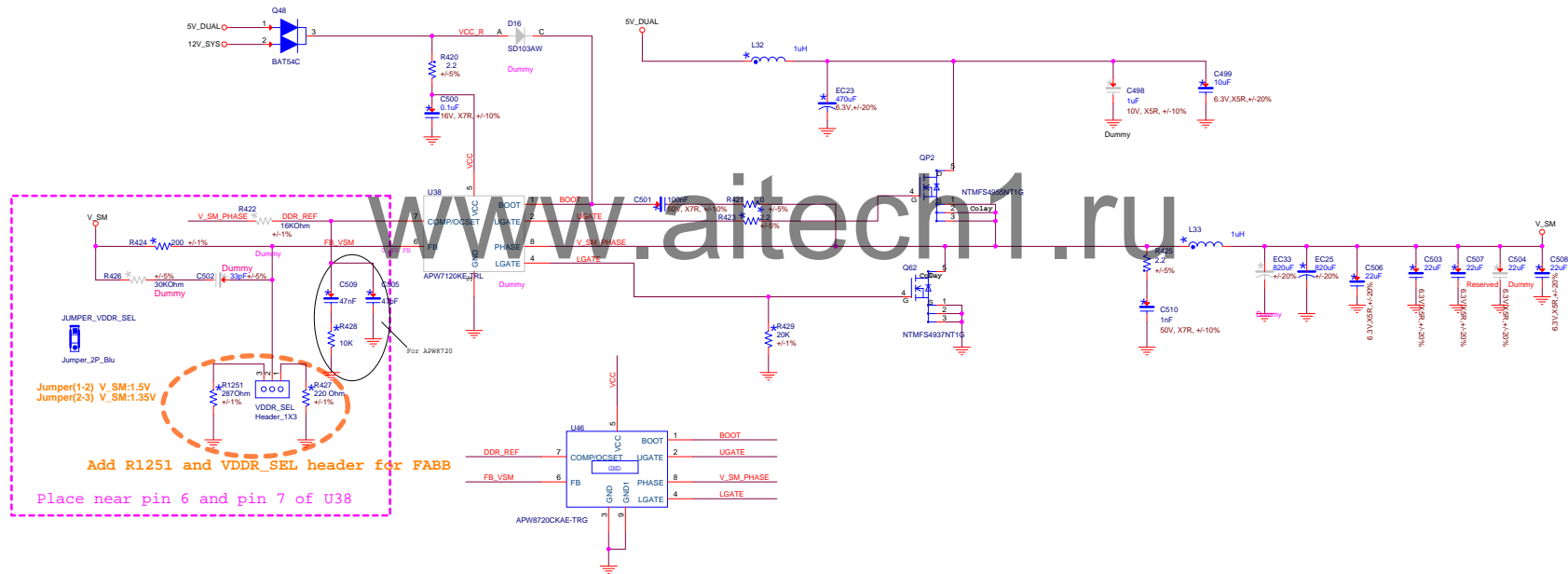
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Title			
5V_DUAL/3D3V_DUAL			
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Max=40A
27A in design guide



Output voltage: +0.75VRUN +/-5%
Output current: 1.5A





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FOXCONN PCEG

Title		
Vcore Driver		
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